User Manual

APM32F003x4x6

Arm® Cortex® -M0+ based 32-bit MCU

Version: V1.6

Contents

1 Introduction and Document Description Rules

1.1 Introduction

This reference manual provides application developers with all the information about how to use MCU (micro-controller) system architecture, memory and peripherals.

For information about Arm® Cortex® -M0+ core, please refer to Arm® Cortex® -M0+ technical reference manual; please refer to the corresponding datasheet for detailed data such as model information, dimension and electrical characteristics of the device; for all MCU series models, please refer to the corresponding data manual for memory mapping, peripheral existence and their number.

1.2 Document description rules

1.2.1 Full Name and Abbreviation Description of Terms

Table 1 R/W Abbreviation and Description

R/W	Description	Abbreviation
read/write	Software can read and write this bit.	R/W
read-only	Software can only read this bit.	R
write-only	Software can only write this bit, and after reading this bit, the reset value will be returned.	W
read/clear	The software can read this bit and clear it by writing 1. Writing 0 has no effect on this bit.	RC_W1
read/clear	The software can read this bit and clear it by writing 0. Writing 1 has no effect on this bit.	RC_W0
read/clear by read	The software can read this bit, reading this bit will automatically clear it to 0, and writing this bit is invalid.	RC_R
read/set	The software can read and set this bit, and writing 0 has no effect on this bit.	R/S
read-only write trigger	The software can read this bit and writing 0 or 1 can trigger an event but has no effect on the value of this bit.	RT_W
toggle	The software can flip this bit only by writing 1, and writing 0 has no effect on this bit.	T

2 System Architecture

2.1 Full Name and Abbreviation Description of Terms

Table 2 Full Name and Abbreviation Description of Terms

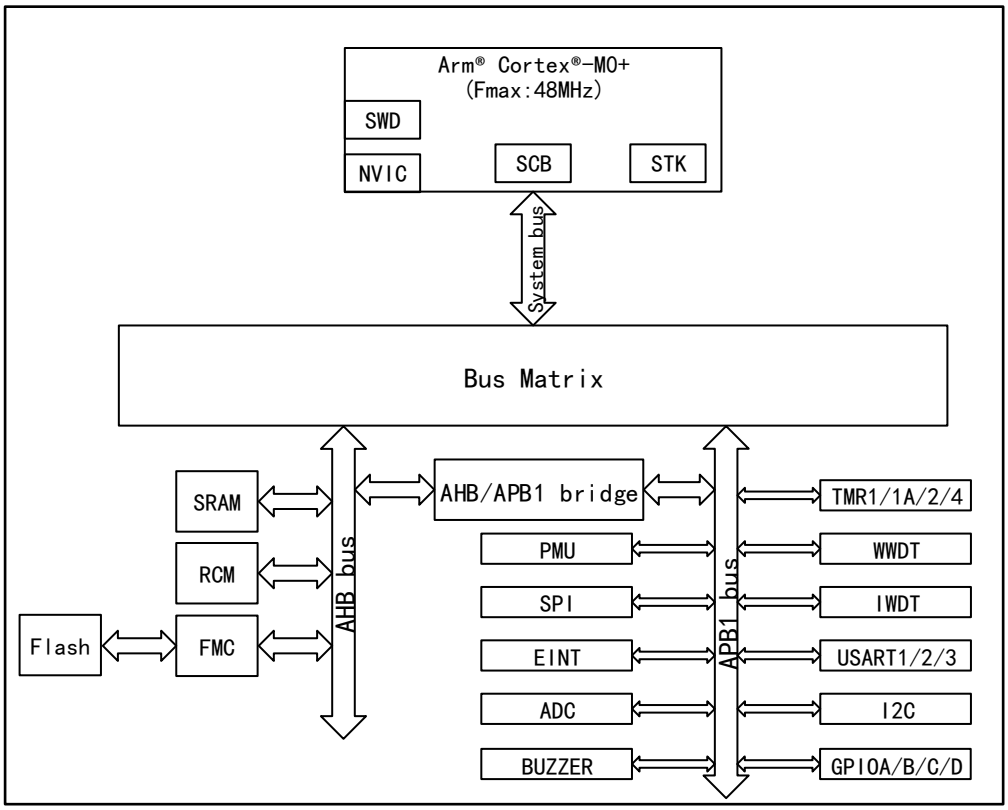
Full name in English	English abbreviation
Advanced High-Performance Bus	AHB
Advanced Peripheral Bus	APB

2.2 System architecture block diagram

The main system consists of one driving unit and three passive units. The driving unit connects the system bus (S-bus) of Arm® Cortex®-M0+ core. The three passive units are internal SRAM, internal flash memory and bridge from AHB to APB, and the bridge connects all APB devices.

These are connected through a multi-level AHB bus architecture, as shown in the figure below:

Figure 1 System Architecture of APM32F003x4x6 Series Products



Note: Different models of products contain different numbers of modules. Please refer to the data manual for details.

2.3 Memory mapping

The memory mapping address is totally 4GB address. The assigned addresses include the core (including core peripherals), on-chip Flash (including main memory area, system memory area and option bytes), on-chip SRAM, and bus peripherals (including AHB and APB peripherals). Please refer to the data manual of the corresponding model for specific information of various addresses.

2.3.1 Embedded SRAM

Built-in static SRAM. It can access by byte, half word (16 bits) or full word (32 bits). The start address of SRAM is 0x2000 0000.

3 Flash Memory

This chapter mainly introduces the storage structure, read, erase, write, read/write protection, unlock/lock characteristics of Flash, and the involved register functional description.

3.1 Full Name and Abbreviation Description of Terms

Table 3 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Flash Memory Controller	FMC

3.2 Main characteristics

(1) Flash memory structure

- Contain main memory area and information block
- The capacity of main memory area is up to 32KB
- The information block is divided into system memory area and option byte area
- The capacity of the system memory area is 1KB, for storing 96-bit unique UID, and main memory area capacity information
- The capacity of the option byte area is 24B

(2) Functional description

- Read Flash
- Page/Mass erase Flash
- Write Flash
- Read/White protection Flash
- Configure option bytes

3.3 Flash memory structure

Table 4 Flash Memory Structure of APM32F003x4x6 Series Products

Block	Name	Address area	Size (bytes)
Main memory area	Page 0	0x0000 0000–0x0000 03FF	1K
Main memory area	Page 1	0x0000 0400–0x0000 07FF	1K
Main memory area	Page 2	0x0000 0800–0x0000 0BFF	1K
Main memory area	Page 3	0x0000 0C00–0x0000 0FFF	1K
Main memory area	…	…	…
Main memory area	Page 31	0x0000 7C00–0x0000 7FFF	1K

Block	Name	Address area	Size (bytes)
Information block	System memory area	0x0002 0000–0x0002 03FF	1K
Information block	Option byte	0x0002 0400–0x0002 07FF	24

Note: The number of pages in the main memory block of APM32F003x4x6 series products is related to the Flash capacity of specific product.

3.4 Flash memory functional description

Describe the operation of main memory and information block (including system memory area and option byte), including read, write, erase and read/write protection.

Reading Flash includes main memory block and information block, while the erase, write, read/write is introduced separately; the system memory area has been written before the product leaves the factory and cannot be modified by the user. The erase, write, and read/write protection of the module will not be introduced.

3.4.1 Read Flash

Flash memory can be directly addressed and reading Flash is affected by the following configuration:

Latency

The number of wait states should be configured for different system clocks:

- 0 wait state: 0<system clock≤24MHz
- 1 wait state: 24MHz<system clock≤48MHz

Prefetch buffer

It can improve the reading speed and the prefetch buffer will be automatically opened while it is reset; the read interface with prefetch buffer is 2×64 bits for APM32F003x4x6 series. It can be turned on or turned off only when the system clock is consistent with AHB clock and is less than 24MHz.

Half-cycle access

When the power consumption needs to be optimized, half-cycle access can be used; at this time, the system clock and AHB clock are consistent, and the system clock is 8MHz or less than 8MHz, then half-cycle access to Flash can be used; otherwise, it must be turned on.

3.4.2 Main memory block

3.4.2.1 Main memory block of erase

FMC supports page erase and mass erase (erase all) to initialize the contents of the main memory area to high level (the data is represented as 0xFFFF). Before writing to Flash, users are advised to erase the write address page. If the data of write address is not 0xFFFF, a programming error will be triggered.

Main memory page erase

Page erase is an independent erase according to the main memory area page selected by the program, which will not have any impact on the page not selected for erasure.

After the correct page erase (or flash write operation) is completed, OCF of FLASH_STS register will be set. If OCIE interrupt is enabled, an operation completion interrupt will be triggered. Users need to pay attention that the page selected for erasure must be a valid page (the valid address of the main memory area and the address not write-protected).

Main memory mass erase

The mass erase operation will erase all the contents in the main storage area of Flash, and the mass erase operation will erase all the data in the main memory area, so the users need to pay special attention when using it to avoid the loss of important data caused by misoperation.

3.4.2.2 Main memory block of write

FMC supports the writing of 16-bit (half word) data in the main memory area. You can select Debug, BootLoader, program running in SRAM, and directly reading the erased page to judge whether the erasing is successful.

In order to ensure correct writing, it is necessary to check whether the destination address has been erased before writing; if it is not erased, the written data will be invalid and PEF bit of FLASH_STS register will be set to "1". If the destination address has write protection, the written data is invalid and a write protection error will be triggered (WPEF bit of FLASH_STS is set to "1").

3.4.2.3 Main memory block of read/write protection

Read/Write protection of the flash is used to prevent invalid reading/modification of the main memory area code or data, and it is controlled by the read/write protection configuration byte of option byte. For APM32F003x4x6 series products, the basic unit of read/write protection is 4 pages (i.e. 4KBytes).

Read protection

Internal Flash protection level can be set by modifying the value of option byte

READPROT. The debugger is always connected to JTAG/SWD interface to set read protection, which takes effect after power-on reset; otherwise, it will not take effect after the system is powered on and reset. When the READPROT value is any value except 0xA5, read protection is enabled and the content of main memory block cannot be read; when the READPROT value is 0xA5, the protection is removed and the content of main memory block can be read; when the read protection is removed, a main memory mass erase operation will be triggered to prevent illegal read after the protection is degraded.

Write protection

Write protection control can be conducted for the corresponding page of the main memory block by configuring the value of write protection option byte WRP0/1/2/3. After the write protection is turned on, the content on the corresponding page of the main memory area cannot be modified in any way.

3.4.2.4 Unlock/Lock main memory block

FLASH_CTRL1 of the reset FMC will be locked by hardware, then FLASH_CTRL1 cannot be directly written, and the corresponding value must be written to FLASH_KEY according to the correct sequence to unlock FMC.

Keyword 1=0x45670123

Keyword 2=0xCDEF89AB

The wrong writing sequence or wrong value will cause the program to enter the hardware wrongly. At this time, FMC will be locked, and all FMC operations will be invalid until it is reset next time. The users can also lock FMC through software by writing "1" to LOCK bit of the control register 2 (FLASH_CTRL2).

In each Flash programming operation, the users must follow the steps of "Flash unlock - program by user - Flash lock", so as to avoid the risk that user code/data is accidentally modified due to the Flash unlocking after the Flash programming operation.

3.4.3 Option byte

3.4.3.1 Erase option byte

It supports the erase function. After erasing of the correct option byte, it needs to be reset to take effect.

Configuration steps

(1) Check BUSYF bit of FLASH_STS register to confirm no other flash operation is ongoing;
(2) Set OBWEN bit in FLASH_ CTRL2 register;
(3) Set OBE bit in FLASH_ CTRL2 register;
(4) Set STA bit in FLASH_ CTRL2 register;

(5) Wait for BUSYF to be reset;
(6) Read out the erased option byte and verify it.

3.4.3.2 Write option byte

9 configurable bytes of option bytes all support writing function. After the option byte is configured, it needs to be reset to take effect.

Configuration steps

(1) Check BUSYF bit of FLASH_STS register to confirm no other flash operation is ongoing;
(2) Set OBWEN bit in FLASH_CTRL2 register;
(3) Set OBP bit in FLASH_CTRL2 register;
(4) Write the half word to be programmed to the specified address;
(5) Wait for BUSYF to be reset;
(6) Read the written value and verify it.

3.4.3.3 Option byte of write protection

By default, the option byte is always readable and write protected. To perform write operation (program/erase) for the option byte block, first write the correct key sequence (the same as that of locking) in FLASH_OBKEY, and then allow the write operation of option byte block; the OBWEN bit of FLASH_CTRL2 register indicates write enabled; clear this bit and write operation will be disabled.

3.4.3.4 Unlock/Lock option byte

After the system reset, the option byte is locked by default. Only when the option byte is unlocked correctly, can it be modified. To unlock the option byte, the keyword shall be written to the FLASH_OBKEY register to unlock. The option byte does not support "software lock". The user should pay special attention to that every time the value of the option byte is modified, the system must be reset to make it take effect.

3.5 Option byte register functional description

The option byte provides some optional functions for users, and it mainly consists of 8 configurable bytes and corresponding complementary codes. Every time the system is reset, the option byte area will be reloaded to the FLASH_OBCS and FLASH_WRTPROT registers (the option byte will only take effect each time they are reloaded to FMC). In the process of reloading, if a certain configurable byte does not match its inverse code, an option byte error (OBE bit of FLASH_OBCS register is set to "1") will be triggered, and this byte will be set to "0xFF". The information of 24 bytes in the option byte area is shown in the table below.

Table 5 Option Bytes

Address	Option byte	Initial value	R/W	Functional Description
0x0002 0400	READPROT	0xA5	R/W	Read protection configuration
0x0002 0401	nREADPROT	0x5A	R	READPROT complementary code
0x0002 0402	USER	0xFF	R/W	User option byte Bit 0: WWDTSW 0: Hardware watchdog 1: Software watchdog Bit 1: WWDTRST 0: Reset is generated in HALT mode when the window watchdog is valid 1: No reset is generated in HALT mode when the window watchdog is valid Bit 2: IWDTSW 0: Hardware activates the independent watchdog 1: Software activates the independent watchdog Bit 3: LIRCEN 0: LIRC clock can be taken as CPU clock source 1: LIRC clock cannot be taken as CPU clock source Bit 4: HIRCTRIM 0: HIRCTRIM register has 4-bit adjustment value 1: HIRCTRIM register has 3-bit adjustment value [5:7]: Reserved
0x0002 0403	nUSER	0x00	R	USER complementary code
0x0002 0404	Data0	0xFF	R/W	User data byte 0
0x0002 0405	nData0	0x00	R	Data0 complementary code
0x0002 0406	Data1	0xFF	R/W	User data byte 1
0x0002 0407	nData1	0x00	R	Data complementary code
0x0002 0408	WRP0	0xFF	R/W	Write protection configuration 0
0x0002 0409	nWRP0	0x00	R	WRP0 complementary code
0x0002 040A	WRP1	0xFF	R/W	Write protection configuration 1
0x0002 040B	nWRP1	0x00	R	WRP1 complementary code
0x0002 040C	WRP2	0xFF	R/W	Write protection configuration 2
0x0002 040D	nWRP2	0x00	R	WRP2 complementary code
0x0002 040E	WRP3	0xFF	R/W	Write protection configuration 3

Address	Option byte	Initial value	R/W	Functional Description
0x0002 040F	nWRP3	0x00	R	WRP3 complementary code
0x0002 0410	AFR	-	R/W	Multiplex mapping option x of bit x, namely, AFRx. Multiplex mapping option 0: 0: Port C5 is multiplexed to TMR2_CH1; Port C6 is multiplexed to TMR1_CH1; Port C7 is multiplexed to TMR1_CH2 1: The mapping option is invalid, and it is multiplexed by default Multiplex mapping option 1: 0: Port A3 is multiplexed to SPI_NSS; Port D2 is multiplexed to TMR2_CH3 1: The mapping option is invalid, and it is multiplexed by default Multiplex mapping option 2: Reserved Multiplex mapping option 3: 0: Port C3 is multiplexed to TLI 1: The mapping option is invalid, and it is multiplexed by default Multiplex mapping option 4: 0:: Port B4 is multiplexed to ADC_ETR; Port B5 is multiplexed to TMR1_BKIN 1: The mapping option is invalid, and it is multiplexed by default Multiplex mapping option 5: 0: Port D5 is multiplexed to TMR1A_CH1N; Port D6 is multiplexed to TMR1A_CH2N 1: The mapping option is invalid, and it is multiplexed by default Multiplex mapping option 6: Reserved Multiplex mapping option 7: 0: Port C3 is multiplexed to TMR1_CH1N; Port C4 is multiplexed to TMR2_CH2N 1: The mapping option is invalid, and it is multiplexed by default

Address	Option byte	Initial value	R/W	Functional Description
				Note: More than one remapping option cannot be enabled on the same port (e.g. AFR0 and AFR1 cannot be enabled at the same time)
0x0002 0411	nAFR	-	R	AFR complementary code
0x0002 0412	Reserved			
0x0002 0413				
0x0002 0414	HXTCNT	0xFF	R/W	Bit [0:7]: HXTCNT 0x1E: 0.5 HXT cycles 0x2D: 8 HXT cycles 0x4B: 128 HXT cycles 0xFF: 2048 HXT cycles
0x0002 0415	nHXTCNT	0x00	R	HXTCNT complementary code
0x0002 0416	CLOCK_OPTION	0xFF	R/W	User option byte Bit [0:1]: WUPTDIV 00: 4 MHz to 128 kHz prescaler 01: 8 MHz to 128 kHz prescaler 1x: 16 MHz to 128 kHz prescaler Bit 2: WUPTLIRC 0: Select HXT frequency divider as clock source 1: Select LSI frequency divider as clock source Bit 3: EXTCLK 0: External clock signal on OSCIN 1: External crystal connected to OSCIN/OSCOUT [4:7]: Reserved
0x0002 0417	nCLOCK_OPTION	0x00	R	CLOCK_OPTION complementary code

Note: When the configurable byte and its complementary code value are "0xFF", the match will not be verified in the reloading process

3.6 Register address mapping

Base address: 0x4001 1000

Table 6 Register Address Mapping

Register name	Description	Offset address
FLASH_CTRL1	Control register 1	0x00
FLASH_KEY	Key register	0x04
FLASH_OBKEY	Option byte key register	0x08
FLASH_STS	State register	0x0C

Register name	Description	Offset address
FLASH_CTRL2	Control register 2	0x10
FLASH_ADDR	Address register	0x14
FLASH_OBCS	Option byte control/state register	0x1C
FLASH_WRTPROT	Write protection register	0x20
FLASH_LPM	Low-power mode register	0x24
FLASH_TPO	Flash tpower_on register	0x28

3.7 Register functional description

3.7.1 Control register 1 (FLASH_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0030

Field	Name	R/W	Description
2:0	LATENCY	R/W	Latency Status Configure 000: 0 wait state, 0<system clock≤24MHz 001: 1 wait state: 24MHz<system clock≤48MHz Others: Reserved
3	HCAEN	R/W	Flash Half Cycle Access Enable 0: Disable 1: Enable
4	PBEN	R/W	Prefetch Buffer Enable 0: Disable 1: Enable
5	PBSF	R	Prefetch Buffer Status Flag 0: In closed state 1: In open state
31:6	Reserved		

3.7.2 Key register 1 (FLASH_KEY)

Offset address: 0x04

Reset value: 0xXXXX XXXX

Field	Name	R/W	Description
31:0	KEY	W	FMC Key Writing the keys represented by these bits can unlock FMC. These bits can only perform write operation, and 0 is returned when read operation is performed.

3.7.3 Option byte key register (FLASH_OBKEY)

Offset address: 0x08

Reset value: 0x03FF FFFC

The reset value of the register is related to the value written in the option byte; the reset value of OBE bit is related to the result of comparison between the loaded option byte and its inverse code.

Field	Name	R/W	Description
31:0	KEY	W	Option Byte Key Writing the keys represented by these bits can unlock the option byte write operation. These bits can only perform write operation and 0 is returned when read operation is performed.

3.7.4 State register (FLASH_STS)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	BUSYF	R	Busy Flag This bit indicates that a flash operation is in progress. These bits can only perform write operation, and 0 is returned when read operation is performed.
1	Reserved		
2	PEF	R/W	Programming Error Flag This bit will be set by software when the value before the address is edited is not "0xFFFF".
3	Reserved		
4	WPEF	R/W	Write Protection Error Flag This bit will be set by hardware when programming the write protection address in FLASH.
5	OCF	R/W	Operation Complete Flag This bit will be set by hardware when read/write operation in FLASH is completed.
31:6	Reserved		

3.7.5 Control register 2 (FLASH_CTRL2)

Offset address: 0x10

Reset value: 0x0000 0080

Field	Name	R/W	Description
0	PG	R/W	Program Set this bit to 1 to program Flash.
1	PAGEERA	R/W	Page Erase Set this bit to 1 to erase the page
2	MASSERA	R/W	Mass Erase Set this bit to 1 to erase the mass.
3	Reserved		
4	OBP	R/W	Option Byte Program Set this bit to 1 to program the option byte.
5	OBE	R/W	Option Byte Erase Set this bit to 1 to erase the option byte.

Field	Name	R/W	Description
6	STA	R/W	Start Erase This bit can be only set to 1 by software, and can be reset by clearing BUSYF bit of STS register.
7	LOCK	R/W	Lock This bit can be written to 1 only, and when it is set to 1, it means that Flash and CTRL2 registers are locked.
8	Reserved		
9	OBWEN	R/W	Option Byte Write Enable When this bit is set to 1, the option byte can be programmed.
10	ERRIE	R/W	Error interrupt Enable 0: Disable interrupt 1: Enable interrupt When PEF=1 or WPEF=1 for the STS register, set this bit to generate an interrupt.
11	Reserved		
12	OCIE	R/W	Operation Complete Interrupt Enable 0: Disable operation completion interrupt 1: Enable operation completion interrupt When OCF=1 for STS register, set this bit to generate an interrupt.
31:13	Reserved		

3.7.6 Address register (FLASH_ADDR)

Offset address: 0x14

Reset value: 0x0000 0000

The register is changed to currently/finally used address by hardware; in page erase, the register needs to be configured by software.

Field	Name	R/W	Description
31:0	ADDR	W	Flash Address In programming operation, the bit is written to the address to be programmed; in page erase, this bit is written to the page to be erased.

3.7.7 Option bye control/state register (FLASH_OBCS)

Offset address: 0x1C

Reset value: 0x03FF FFFC

The reset value of the register is related to the value written in the option byte; the reset value of OBE bit is related to the result whether the value of the loaded option byte is consistent with its inverse code.

Field	Name	R/W	Description
0	OBE	R	Option Byte Error 1: The loaded option byte does not match its complementary code. The option byte and its complementary code are forced to write to 0xFF
1	READPROT	R	Read Protect 1: Indicate that the flash memory is in read protection state

Field	Name	R/W	Description
2	WWDTSW	R	WWDT Switch 0: Hardware activates the window watchdog 1: Software activates the window watchdog
3	WWDTRST	R	WWDT Reset This bit controls the window watchdog to generate reset in HALT mode. 0: Generate 1: Not generate
4	IWDTSW	R	IWDT Switch 0: Hardware activates the independent watchdog 1: Software activates the independent watchdog
5	LIRCEN	R	LIRC Enable 0: LIRC clock can be taken as CPU clock source 1: LIRC clock cannot be taken as CPU clock source
6	HIRCTRIM	R	HIRC Trim This bit controls the bit number of adjustment values that the HIRCTRIM register has. 0: 4 bits 1: 3 bits
9:7	Reserved		
17:10	DATA0	R	Data0
25:18	DATA1	R	Data1
31:26	Reserved		

3.7.8 Write protection register (FLASH_WRTPROT)

Offset address: 0x20

Reset value: 0xFFFF FFFF

Field	Name	R/W	Description
31:0	WRTPROT	R	Write Protect 0: Valid 1: Invalid

3.7.9 Low-power mode register (FLASH_LPM)

Offset address: 0x24

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	HALT	R/W	Flash is Power-down in Halt mode This bit is set to 1 or cleared to 0 by software. 0: When MCU is in halt mode, Flash is power-down. 1: When MCU is in halt mode, Flash is in working state.
1	AHALT	R/W	Flash is Power-down in Active-halt mode This bit is set to 1 or cleared to 0 by software. 0: When MCU is in Active-halt mode, Flash is in working state. 1: When MCU is in Active-halt mode, Flash is power-down.

Field	Name	R/W	Description
31:2	Reserved		

3.7.10 Flash tpower_on register (FLASH_TPO)

Offset address: 0x28

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	TPO	R/W	The t_{su} of Flash in Power-down mode When Flash starts from power-down mode, it needs to wait for 2us to run normally.
31:8	Reserved		

4 Power Management Unit (PMU)

4.1 Full Name and Abbreviation Description of Terms

Table 7 Full Name and Abbreviation Description of Terms

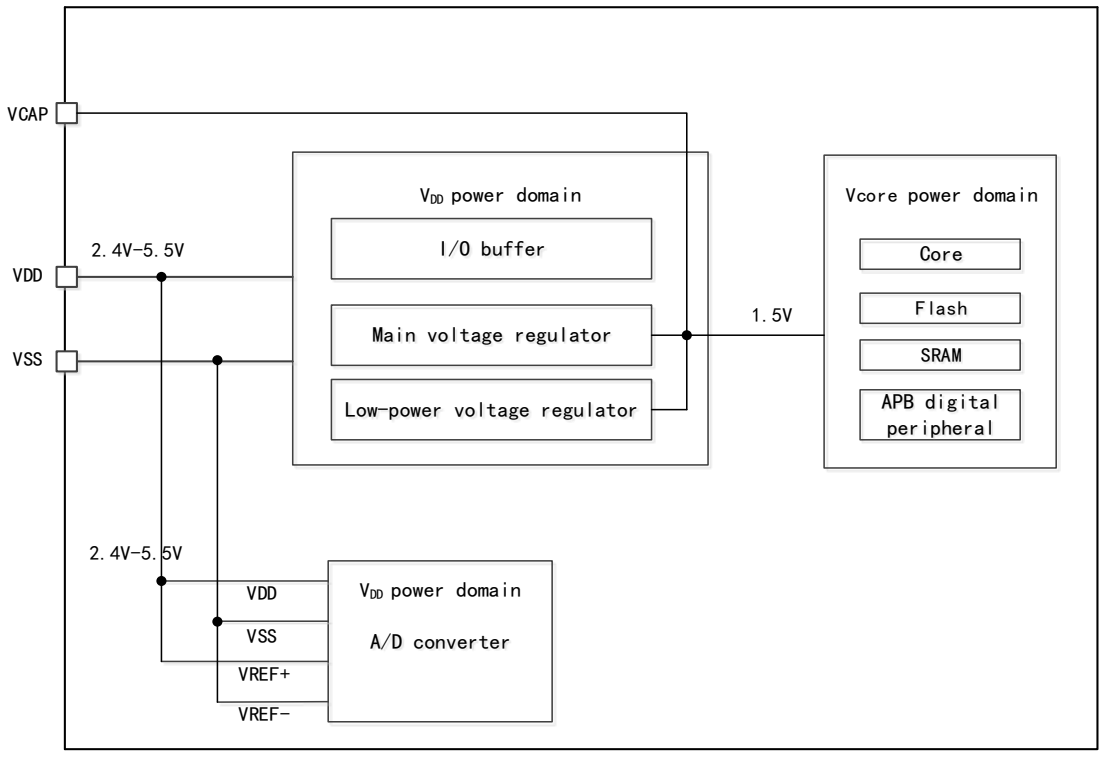
Full name in English	English abbreviation
Power On Reset	POR
Power Down Reset	PDR

4.2 Introduction

The power supply is the foundation for stable operation of a system, with working voltage of 2.4~5.5V, and 1.5V power supply can be provided through the built-in voltage regulator to digital peripherals.

4.3 Structure block diagram

Figure 2 Power Supply Control Structure Block Diagram



4.4 Functional Description

4.4.1 Power domain

The power domain of the product includes: V_{DD} power domain, and V_{Core} power domain.

4.4.1.1 V_{DD} power domain

V_{DD}/ V_{SS} pin can supply power for internal main voltage regulator (MVR), internal low-power voltage regulator (LPVR) and I/O ports, and the voltage range is 2.4~5.5V.

4.4.1.2 V_{Core} power domain

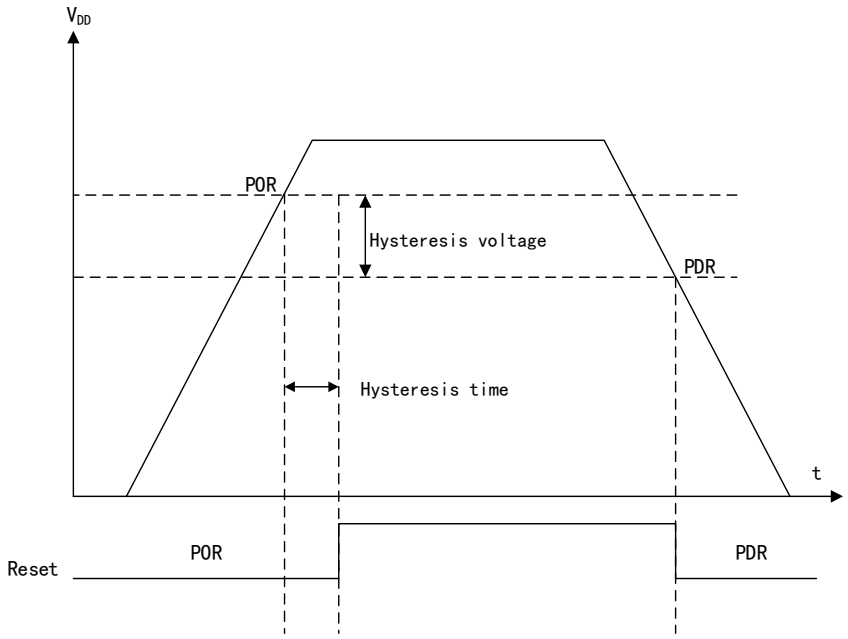
The main voltage regulator and low-Power voltage regulator supply power for the core, FLASH, RAM and digital peripherals, and the power supply voltage is 1.5V.

4.5 Power Management

4.5.1 Power-on/power-down reset (POR and PDR)

When the V_{DD} is detected to be lower than the threshold voltage V_{POR} and V_{PDR}, the chip will automatically remain in the reset state. The waveform diagrams of power-on reset and power-down reset are as follows. For POR, PDR, hysteresis voltage and hysteresis time, please refer to the "Datasheet".

Figure 3 Power-on Reset and Power-down Reset Oscillogram



4.5.2 Power control

4.5.2.1 Reduce the power in low-power mode

There are four low-power modes: wait mode, fast active-halt mode, slow active-halt mode, and halt mode. The power is reduced by closing the core and clock source and setting the voltage regulator.

Table 8 Main Characteristics of Four Low-power Modes

Mode	Wakeup and trigger event	CPU	Oscillator	Main voltage regulator	Peripheral
Wait	All internal interruupts or external interrupts, reset	Off	On	On	On (1)
Fast active-halt	WUPT or external (2) interrupt, reset	Off	Off except LIRC (or HXT)	On	Only WUPT and IWDT (if they have been activated)
Slow active-halt	WUPT or external (2) interrupt, reset	Off	Off except LIRC	Off (the low-power voltage regulator is on)	Only WUPT and IWDT (if they have been activated)
Stop	External (2) interrupt, reset	Off	Off	Off (the low-power voltage regulator is on)	Off

Note: 1. If peripheral clock is not turned off

2. Include interrupt of communication peripheral (SPI, I2C) (see the interrupt vector table)

Wait mode

Table 9 Characteristics of Wait Mode

Characteristics	Description
Enter	Enter the wait mode by executing WFI instruction
Wakeup	Wake up by any interrupt
During waiting	The core stops running, peripherals and interrupt controllers remain running, and all registers, RAM and defined clock configurations remain unchanged
Wakeup delay	None

Stop mode

Table 10 Characteristics of Halt Mode

Characteristics	Description
Enter	Enter the halt mode by executing HALT instruction
Wakeup	Wake up by internal interrupt
Stop	The master clock, CPU and peripherals stop running, the contents of all registers and RAM remain unchanged, the clock configuration remains unchanged by default, and the low voltage regulator is in working state
Wakeup delay	Wakeup time of master clock + voltage regulator wakeup time from low-power mode

Active-halt

Table 11 Characteristics of Active-halt Mode

Characteristics	Description
Enter	First enable WUPT and then enter the active-halt mode by executing HALT instruction
Wakeup	Wake up automatically by internal event
Active-halt	The main oscillator, CPU and peripherals stop running. If WUPT and IWDT are enabled, only LIRC and HXT are running to drive the counters of WUPT and IWDT.
Wakeup delay	Wakeup time of master clock + voltage regulator wakeup time from low-power mode (FLASH is always working, which can reduce the wakeup time)

4.5.2.2 Reduce the power in run mode

In run mode, the power can be reduced by reducing the system clock, turning off unused peripherals and turning off all unused analog function blocks.

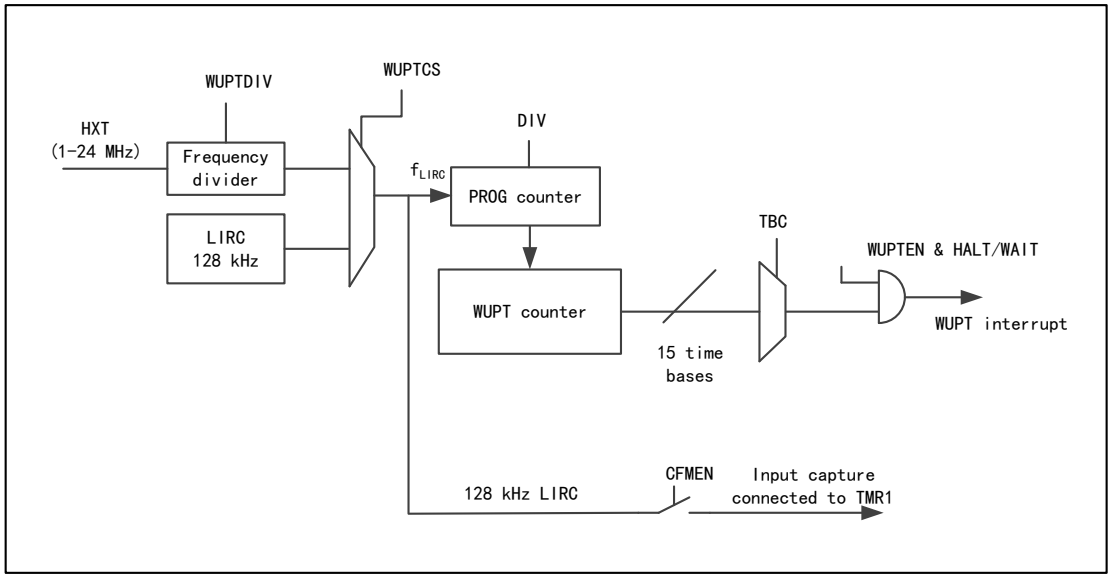
5 Auto Wakeup (WUPT)

5.1 Introduction

WUPT can provide an internal wakeup time reference when MCU enters low-power active-halt mode. The clock of the time reference is provided by the internal low-speed RC oscillator clock (LIRC) or the HXT crystal oscillator clock of prescaler.

5.2 Structure block diagram

Figure 4 WUPT Clock Block Diagram



5.3 Functional Description

5.3.1 WUPT configuration process

- Set CFMEN bit of the configuration register WUPT_CSTS to 1 to connect LIRC to the input capture channel 1 of TMR1
- Define appropriate prescaler value by DIV[5:0] bit of the configuration register WUPT_DIV
- Select required automatic wakeup delay through TBC[3:0] bit of the configuration register WUPT_TBC
- Enable WUPT function through WUPTEN bit of the configuration register WUPT_CSTS
- Execute HALT instruction

5.3.2 LIRC clock frequency detection

In order to obtain accurate automatic wakeup time interval or buzzer output, it is necessary to accurately measure the LIRC frequency

The clock frequency detection steps are as follows:

- Set CFMEN bit of the configuration register WUPT_CSTS to 1 to connect LIRC to the input capture channel 1 of TMR1
- Measure the frequency of LIRC through input capture interrupt of the timer

5.3.3 Time base selection

The time interval of WUPT depends on: output column of counter given by TBC [3:0] bit and prescaler factor given by DIV [5:0] bit. 15 non-overlapping time intervals can be defined, as shown in the following table:

Table 12 TBC[3:0] Selection

TBC[3:0]	Time interval	DIV range
0001	$2/f_{LIRC}$-$64/f_{LIRC}$	2 to 64
0010	$2\times32/f_{LIRC}$-$2\times64/f_{LIRC}$	32 to 64
0011	$2\times2\times32/f_{LIRC}$ -$2^2\times64/f_{LIRC}$	32 to 64
0100	$2\times2^2\times32/f_{LIRC}$ -$2^3\times64/f_{LIRC}$	32 to 64
…		
1100	$2\times2^{10}\times32/f_{LIRC}$ -$2^{11}\times64/f_{LIRC}$	32 to 64
1101	$2\times2^{11}\times32/f_{LIRC}$ -$2^{12}\times64/f_{LIRC}$	32 to 64
1110	$2^{11}\times130/f_{LIRC}$ -$2^{11}\times320/f_{LIRC}$	26 to 64
1111	$2^{11}\times330/f_{LIRC}$ -$2^{12}\times960/f_{LIRC}$	11 to 64

The user can determine the value of WUPTTBC [3:0] according to the desired time interval, and then select the value of the corresponding DIV [5:0].

5.4 Register address mapping

Table 13 Register Address Mapping

Register name	Description	Offset address
WUPT_CSTS	WUPT control state register	0x00
WUPT_DIV	WUPT asynchronous prescaler register	0x04
WUPT_TBC	WUPT time base selection register	0x08

5.5 Register functional description

5.5.1 WUPT control state register (WUPT_CSTS)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CFMEN	R/W	Measurement Enable 0: Disable 1: Enable
3:1	Reserved		
4	WUPTEN	R/W	Auto-wakeup Enable This bit is set to 1 and cleared to 0 by the software. If the MCU enters the active-halt or wait mode, the automatic wakeup module will be programmed in advance to wake up the MCU after a certain time delay. 0: Disable 1: Enable
5	WUPIF	R/W	Auto-wakeup Interrupt Flag This bit is cleared when performing read operation to WUPT_CSTS register, but write operation is invalid. 0: No automatic wakeup interrupt is generated 1: Automatic wakeup interrupt is generated
31:6	Reserved		

5.5.2 WUPT asynchronous prescaler register (WUPT_DIV)

Offset address: 0x04

Reset value: 0x0000 00C0

Field	Name	R/W	Description
5:0	DIV	R/W	Asynchronous Prescaler Value Select This bit is used to select the prescaler value provided to the counter clock. 00h: 2 divided frequency 01h: 3 divided frequency … 06h: 8 divided frequency … 0Eh: 16 divided frequency 0Fh: 17 divided frequency … 3Eh: 64 divided frequency Note: This register cannot set to the initial reset value (3Fh)
31:6	Reserved		

5.5.3 WUPT time base selection register (WUPT_TBC)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	TBC	R/W	Auto-wakeup Timebase Select This bit is used to define the automatic wakeup interrupt time. 0000: No automatic wakeup interrupt 0001: C=1 0100: C=2 0011: C=2^2

Field	Name	R/W	Description
			0100: $C=2^3$ 0101: $C=2^4$ 0110: $C=2^5$ 0111: $C=2^6$ 1000: $C=2^7$ 1001: $C=2^8$ 1010: $C=2^9$ 1011: $C=2^{10}$ 1100: $C=2^{11}$ 1101: $C=2^{12}$ 1110: $C=5\times2^{11}$ 1111: $C=30\times2^{11}$ C is coefficient; basic duration =$C\times DIV/f_{LIRC}$
31:4	Reserved		

6 Reset and Clock (RCM)

6.1 Full Name and Abbreviation Description of Terms

Table 14 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Reset and Clock Management	RCM
Reset	RST
Power-On Reset	POR
Power-Down Reset	PDR
High Speed External Clock	HXT
High Speed Internal Clock	HIRC
Low Speed Internal Clock	LIRC
Calibrate	CAL
Trim	TRM
Wakeup	WUP
Automatic Wakeup	AWUP
Backup	BAKP
Low Power	LPWR
Clock Security System	CSS
Non Maskable Interrupt	NMI

6.2 Reset functional description (RMU)

The supported reset is divided into two forms, namely, system reset, and power reset.

6.2.1 System reset

6.2.1.1 "System reset" reset source

The reset source is divided into external reset source and internal reset source.

External reset source:

- Low level on NRST pin.

Internal reset source:

- Window watchdog termination count (WWDT reset)
- Independent watchdog termination count (IWDT reset)
- Software reset (SW reset)
- Power-on reset (POR) /Power-down reset (PDR)

- CPU software reset
- EMC reset

A system reset will occur in case of any above event. Besides, the reset event source can be identified by viewing the reset flag bit in RCM_CSTS (control/state register).

Generally speaking, when the system is reset, all registers except the registers in RCM_CSTS (control/state register) reset flag bit and backup area will be reset to the reset state.

Software reset

WWDT reset can be generated by clearing the 7th bit of WWDT_CTRL register of the window watchdog.

CPU software reset

Software reset of CPU can be realized by setting SYSRESETREQ in Arm® Cortex® -M0+ interrupt application and reset control register to "1".

EMC reset

If the important registers do not match their complementary register, a reset will be generated to make the system run again and return to normal.

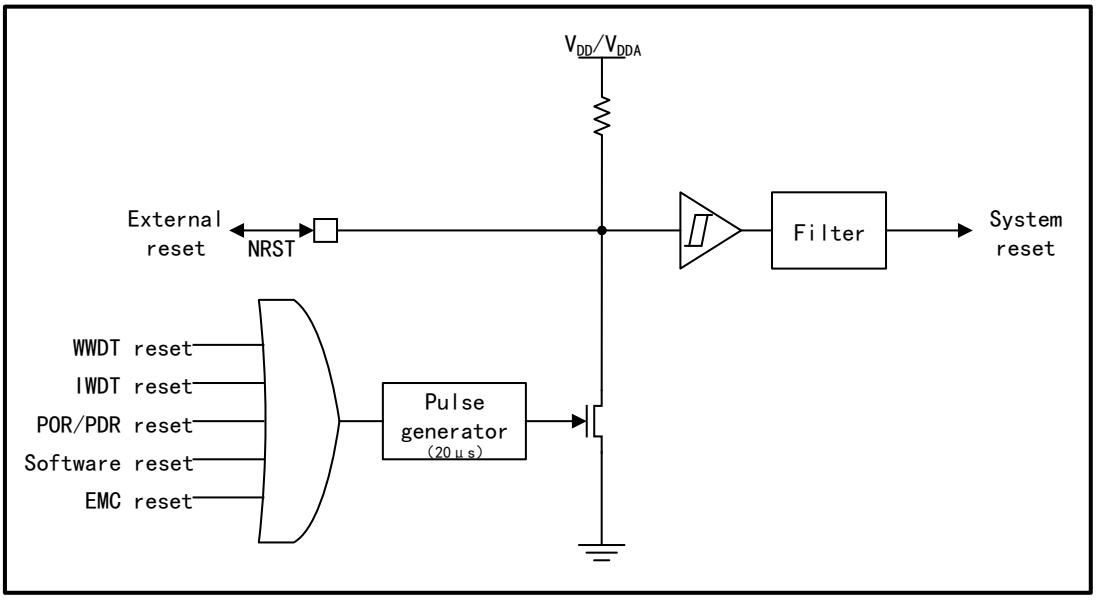
6.2.1.2 "System reset" reset circuit

The reset source is used in the NRST pin, which remains low in reset process.

The internal reset source generates a delay of at least 20μs pulse on the NRST pin through the pulse generator, which causes the NRST to maintain the level to generate reset; the external reset source directly pulls down the NRST pin level to generate reset.

The "system reset" reset circuit is shown in the following figure.

Figure 5 "System Reset" Reset Circuit



6.2.2 Power reset

"Power reset" reset source

"Power reset" reset source is as follows:

- Power-on reset (POR reset)
- Power-down reset (PDR reset)

A power reset will occur in case of any above event.

6.3 Functional description of clock management (CMU)

Clock sources of the whole system are: HXT, HIRC and LIRC. For the characteristics of the clock source, please refer to the relevant chapter of "Electrical Characteristics" in the data manual.

6.3.1 External clock source

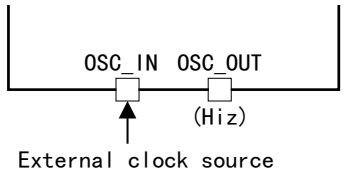
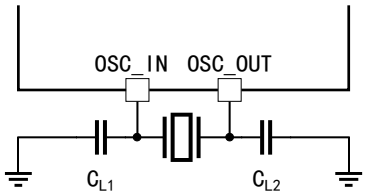
The external clock signal is HXT (higih-speed external clock signal).

There are two kinds of external clock sources:

- External crystal/ceramic resonator
- External clock of user

The hardware configuration of the two kinds of clock sources is shown in the figure below.

Figure 6 HXT Clock Source Hardware Configuration

Clock source	Hardware configuration
External clock	
Crystal /Ceramic resonator	

In order to reduce the distortion of clock output and shorten the start-up stabilization time, the crystal/ceramic resonator and load capacitor must be as close to the oscillator pin as possible. The value of load capacitance (C_{L1}, C_{L2}) must be adjusted according to the selected oscillator.

6.3.1.1 HXT high-speed external clock signal

HXT clock signal is generated by HXT external crystal/ceramic resonator and HXT external clock two kinds of clock sources.

Table 15 Clock Source Generting HXT

Name	Description
External clock source (HXT bypass)	Provide clock to the MCU through OSC_IN pin. The signal can be generated by ordinary function signal transmitter (in debugging), crystal oscillator and other signal generators; the waveform can be square wave, sine wave or triangle wave with 50% duty cycle, and the maximum frequency is up to 24MHz. For hardware connection, it must be connected to OSC_IN pin, ensuring OSC_OUT pin is suspended; for MCU configuration, the user can select this mode by setting EXTCLK bit in option byte and HXTEN bit of RCM_ECC.
External crystal/ceramic resonator (HXT crystal)	The clock is provided to MCU by the resonator, and the resonator includes crystal resonator and ceramic resonator. The frequency range is 1~24MHz. When needing to connect OSC_IN and OSC_OUT to the resonator, it can be enabled and closed by setting the HXTEN bit of RCM_ECC in clock control register. HXTRF bit in RCM_ECC is used to indicate whether the high-speed external oscillator is stable. After startup, the clock is not released until this bit is set to "1" by hardware.

6.3.2 Internal clock source

The internal clock includes HIRC (high-speed internal clock signal) and LIRC (low-speed internal clock signal).

6.3.2.1 HIRC high-speed internal clock signal

HIRC clock signal is generated by internal 48MHz RC oscillator.

The RC oscillator frequency of different chips is different, and that of the same chip may also be different with the change of temperature and voltage; the HIRC clock frequency of each chip has been calibrated to ±1% (25℃, V_{DD}= 3.3V) by the manufacturer before leaving the factory. When the system is reset, the value calibrated by the manufacturer will be loaded to RCM_HIRCTRIM; in addition, the users can further adjust the frequency by setting TRIM in RCM_HIRCTRIM according to the application environment (temperature and voltage) of the site.

HIRCEN bit can be used to indicate whether HIRC RC oscillator is stable. In the clock startup process, HIRC RC output clock is not released until the HIRCRF bit is set to 1 by hardware. HIRC RC can be turned on or off by HIRCEN bit in RCM_ICC.

Compared with HXT crystal oscillator, RC oscillator can provide system clock without any external device; the start time of RC oscillator is shorter than that of HXT crystal oscillator; even after calibration, its clock frequency accuracy is still inferior to that of HXT crystal oscillator.

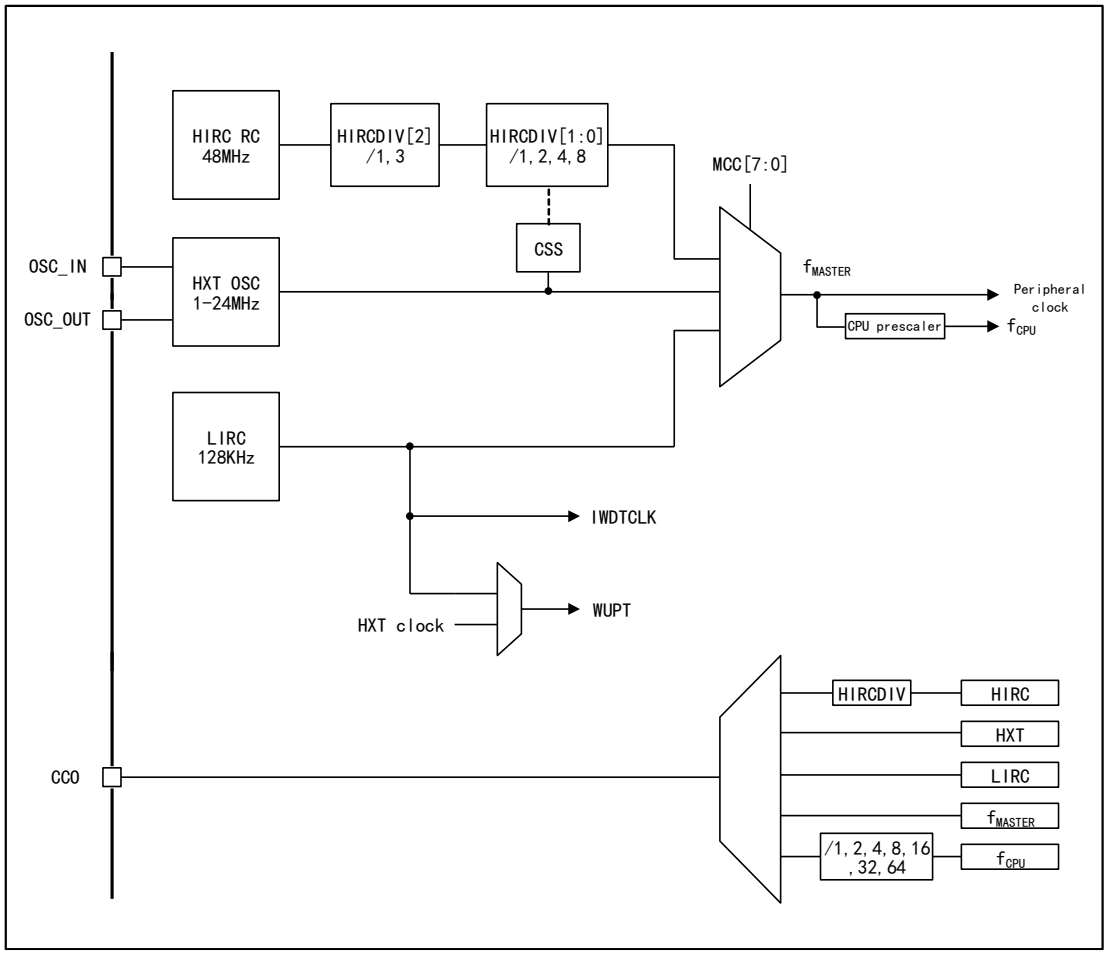
6.3.2.2 LIRC low-speed internal clock signal

LIRC is generated by RC oscillator, and the frequency is about 128kHz (the frequency may change along with the change of temperature and voltage). It can keep running in stop and standby mode and provide clock for independent watchdog and automatic wakeup unit.

LIRC can be turned on or off by LIRCEN bit of RCM_ICC. LIRCRF bit in RCM_ICC indicates whether the low-speed internal oscillator is stable. At startup stage, the clock is not released until this bit is set to "1" by hardware.

6.3.3 Clock tree

Figure 7 APM32F003x4x6 Clock Tree



Note:

(1) When needing to run the peripheral connected to AHB and APB, it is required to turn on the corresponding enable end to make the peripheral get the clock signal.

6.3.4 Clock source selection of CCO

Users can output various clocks through CCO pin, including HXT, HIRC, $f_{HIRCDIV}$, f_{LIRC}, f_{MASTER} and f_{CPU}.

COS[3:0] of the clock output control register (RCM_COC) can select the output clock. See the clock tree for specific clock signal.

When the clock is output, COBF is set and COS bit is write-protected.

Users can disable the clock output function by clearing COEN bit.

6.3.5 Clock source selection of SYSCLK

After reset, the clock controller automatically uses HIRC/8 as the master clock. Once the master clock source is stable, the user can replace the clock source of

the master clock according to the actual needs.

6.3.5.1 Automatic switching of clock source

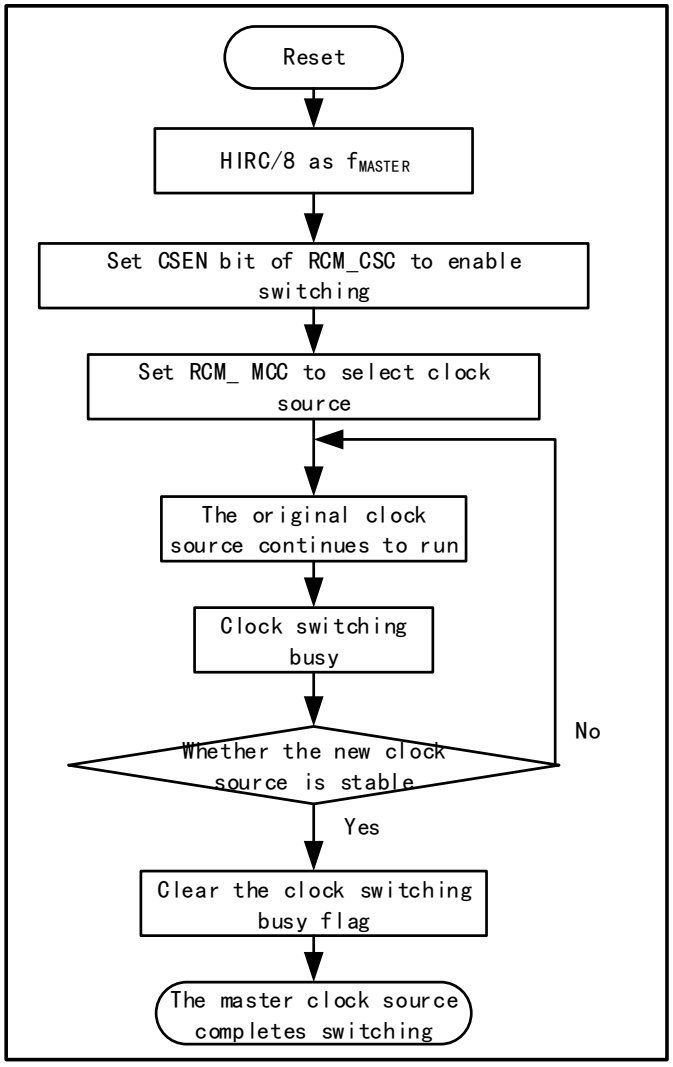
The user does not need to wait for the clock source to be stable, and can continue other operations in the switching process.

(1) Set the CSEN bit in the clock switching control register (RCM_CSC)) to enable switching.

(2) Set the master clock configuration register (RCM_MCC) and select the clock source. The target source oscillator starts, and the original clock source still drives the core and peripherals.

Until the target clock source is stable, the master clock state register (RCM_MCS) is updated to the flag of the target clock source, the MCS bit is cleared and the switching of the clock source is completed. The clock switching interrupt flag is set. If the clock switching interrupt is turned on, an interrupt will be generated.

Figure 8Automatic Switching Flow Chart



6.3.5.2 Manual switching of clock source

Manual switching cannot be completed immediately, but the user can accurately control the occurrence time of the switching.

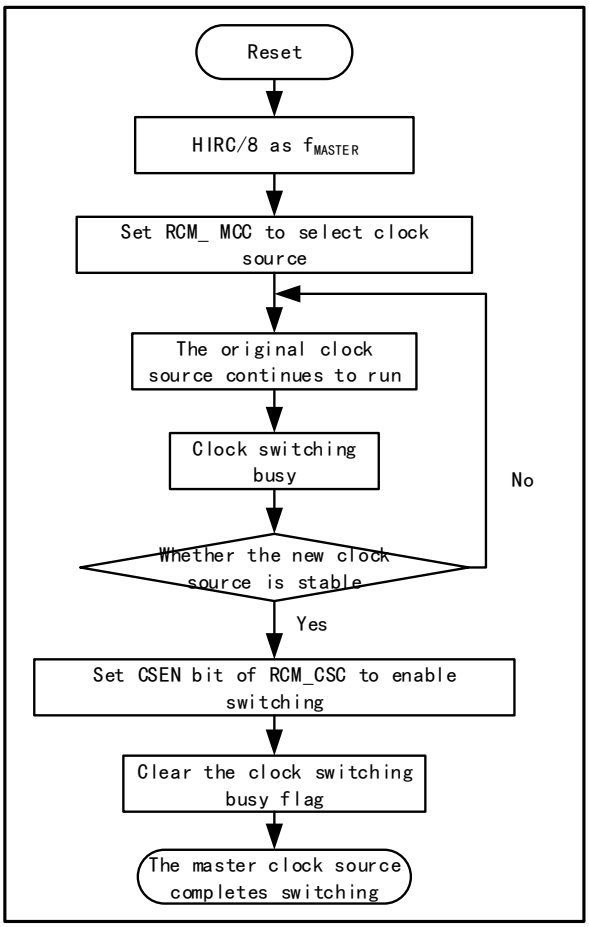
(1) Set the master clock configuration register (RCM_MCC) and select the clock source. The target source oscillator starts, and the original clock source still drives the core and peripherals.

(2) The user needs to wait for the clock source to be stable. Judge whether the clock source is ready through the CSIF flag bit in the register (RCM_CSC).

(3) When the clock is stable, the user can complete switching by setting the CSEN bit in the clock switching control register (RCM_CSC).

If the clock switching fails for some reason, the flag bit CSBF can be cleared by software to reset the current switching operation and the original clock source can be restored through the register RCM_MCC.

Figure 9 Manual Switching Flow Chart



6.3.5.3 Low-speed clock source selection

The low-speed clock source used by the automatic wakeup unit (WUPT) and

IWDT can be selected through the WUPTCS bit of the option byte, which can be frequency division of LIRC or HXT. In order to make the HXT output 128KHz clock signal after frequency division, different frequency division factors need to be set for different HXT crystal oscillators, which can be set through the option byte WUPTDIV [1:0], so as to enable the HXT frequency division to output a 128kHz clock signal.

6.3.6 CPU clock

f_{CPU} is obtained from frequency division of f_{MASTER}, and the division factor is set through the CPUDIV[2:0] of clock prescasler register (RCM_CLKDIV).

6.3.7 CSS clock security system

It is used to monitor whether HXT clock source fails. When HXT is used as the system clock source, if the HXT oscillator has physical failure or other failure problems, the clock security system will be introduced in order to ensure that the MCU can still work normally. When HXT fails, the clock security system will automatically switch the clock to HIRC/24. If the user turns on CSS interrupt, corresponding system protection measures can be taken and a new clock source can be switched in CSS interrupt.

Set the CSSEN bit in clock protection system register RCM_CSS to enable the clock security system. For safety's sake, once CSS is enabled, it cannot be turned off until the next reset.

6.3.7.1 Method of turning on CSS

(1) Turn on HXT crystal;

(2) HXT oscillator is set to quartz crystal;

(3) Enable CSS function.

6.3.7.2 HXT fails when HXT is the master clock source

- The CSSFDIF bit of the register RCM_CSS is set and if CSSFDIE is 1, an interrupt will be generated.
- The HIRC frequency division factor is set to the reset value, and the master clock source is configured. HIRC/24 is the master clock.
- HIRCEN is set and HIRC is turned on; HXTEN is cleared and HXT is turned off.
- The BCEN bit is set to indicate that the auxiliary clock source HIRC/24 is forced to use.
- The user can clear CSSD bit through software, and BCEN bit can only be cleared by reset.

6.3.7.3 HXT fails when HXT is not the master clock source

- The master clock will not switch to the auxiliary clock source.
- HXTEN in the register RCM_ECC is cleared and HXT is turned off.

- The CSSFDIF bit of the register RCM_CSS is set and if CSSFDIE is 1, an interrupt will be generated.

If the master clock is switching to HXT, the CSBF bit of the register RCM_CSC must be cleared before clearing the CSSFDIF bit.

If HXT is selected as the clock output mode by CCOSEL when the failure is detected, HIRC (HIRCDIV) will replace HXT and be automatically forced to be selected as the output clock.

6.4 Register address mapping

Table 16 Register Address Mapping

Register name	Description	Offset address
RCM_ICC	Internal clock control register	0x00
RCM_ECC	External clock control register	0x04
RCM_MCS	Master clock state register	0x0C
RCM_MCC	Master clock configuration register	0x10
RCM_CSC	Clock switching control register	0x14
RCM_CLKDIV	Clock prescaler register	0x18
RCM_APBEN1	APB clock enable register 1	0x1C
RCM_CSS	Clock protection system register	0x20
RCM_COC	Clock output control register	0x24
RCM_APBEN2	APB clock enable register 2	0x28
RCM_HIRCTRIM	Internal high-speed clock adjustment register	0x30
RCM_RSTSTS	Reset state register	0x38
RCM_APBEN3	APB clock enable register 3	0x3C

6.5 Register functional description

6.5.1 Internal clock control register (RCM_ICC)

Offset address: 0x00

Reset value: 0x0000 0001

Field	Name	R/W	Description
0	HIRCEN	R/W	HIRC Clock Enable 0: Turn off internal high-speed clock 1: Turn on internal high-speed clock
1	HIRCRF	R	HIRC Ready Flag 0: HIRC not ready 1: HIRC ready

Field	Name	R/W	Description
2	FWFHEN	R/W	Fast Wakeup from Halt Enable 0: Disable fast wake-up 1: Enable fast wakeup
3	LIRCEN	R/W	LIRC Enable 0: Turn off LIRC 1: Turn on LIRC
4	LIRCRF	R	LIRC Ready Flag 0: LIRC not ready 1: LIRC ready
5	RPOEN	R/W	Regulator Power off in Active Halt Mode Enable 0: Turn on the voltage regulator in Active-halt mode 1: Turn off the voltage regulator in Active-halt mode
31:6	Reserved		

6.5.2 External clock control register (RCM_ECC)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	HXTEN	R/W	HXT Enable 0: Turn off HXT 1: Turn on HXT
1	HXTRF	R	HXT Ready Flag 0: HXT not ready 1: HXT ready
31:2	Reserved		

6.5.3 Master clock state register (RCM_MCS)

Offset address: 0x0C

Reset value: 0x0000 00E1

Field	Name	R/W	Description
7:0	MCS	R	Main Clock Status 0xE1: Indicate HIRC is master clock source 0xD2: Indicate LIRC is master clock source 0xB4: Indicate HXT is master clock source Others: Reserved
31:8	Reserved		

6.5.4 Master clock configuration register (RCM_MCC)

Offset address: 0x10

Reset value: 0x0000 00E1

Field	Name	R/W	Description
7:0	MCC	R/W	Main Clock Configure 0xE1: Configuration HIRC is master clock source 0xD2: Configuration LIRC is master clock source 0xB4: Configuration HXT is master clock source
31:8	Reserved		

6.5.5 Clock switching control register (RCM_CSC)

Offset address: 0x14

Reset value: 0x0000 00XX

Field	Name	R/W	Description
0	CSBF	R/W	Clock Switch Busy Flag 0: The clock does not switch 1: The clock is switching
1	CSEN	R/W	Clock Switch Enable 0: Disable clock switching 1: Enable clock switching
2	CSIE	R/W	Clock Switch Interrupt Enable 0: Disable clock switching interrupt 1: Enable clock switching interrupt
3	CSIF	RC_W0	Clock Switch Interrupt Flag For manual clock switching (CSEN=0): 0: The target clock is not stable 1: The target clock is already stable For automatic clock switching (CSEN=1): 0: Clock switching event does not occur 1: Clock switching event occurs
31:4	Reserved		

6.5.6 Clock prescaler register (RCM_CLKDIV)

Offset address: 0x18

Reset value: 0x0000 0018

Field	Name	R/W	Description
2:0	CPUDIV	R/W	CPU Clock Divider Factor 000: 2 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128

Field	Name	R/W	Description
4:3	HIRCDIV	R/W	HIRC Clock Divider Factor 00: 1 01: 2 10: 4 11: 8
5	HDS	R/W	HIRC Divider Set 0: HIRC/3 1: HIRC
31:6	Reserved		

6.5.7 APB clock enable register 1 (RCM_APBEN1)

Offset address: 0x1C

Reset value: 0x0000 00FF

Field	Name	R/W	Description
0	I2CCEN	R/W	I2C Clock Enable 0: Disable 1: Enable
1	SPICEN	R/W	SPI Clock Enable 0: Disable 1: Enable
2	Reserved		
3	USART1CEN	R/W	USART1 Clock Enable 0: Disable 1: Enable
4	TMR4CEN	R/W	TMR4 Clock Enable 0: Disable 1: Enable
5	TMR2CEN	R/W	TMR4 Clock Enable 0: Disable 1: Enable
6	Reserved		
7	TMR1CEN	R/W	TMR4 Clock Enable 0: Disable 1: Enable
31:8	Reserved		

6.5.8 Clock protection system register (RCM_CSS)

Offset address: 0x20

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CSSEN	R/W	Clock Security System Enable 0: Disable 1: Enable

Field	Name	R/W	Description
1	BCEN	R/W	Backup Clock Enable 0: Disable 1: Enable
2	CSSFDIE	R/W	CSS Fault Detect Interrupt Enable 0: Disable clock protection system fault detection interrupt 1: Enable the clock protection system fault detection interrupt
3	CSSFDIF	R/W	CSS Fault Detect Interrupt Flag 0: HXT clock fault is not detected 1: HXT clock fault is detected
31:4	Reserved		

6.5.9 Clock output control register (RCM_COC)

Offset address: 0x24

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	COEN	R/W	Clock Output Enable 0: Disable 1: Enable
4:1	COS	R/W	Clock Output Select 0000: $f_{HIRCDIV}$ 0001: f_{LIRC} 0010: f_{HXT} 0011: Reserved 0100: f_{CPU} 0101: $f_{CPU/2}$ 0110: $f_{CPU/4}$ 0111: $f_{CPU/8}$ 1000: $f_{CPU/16}$ 1001: $f_{CPU/32}$ 1010: $f_{CPU/64}$ 1011: f_{HIRC} 1100: f_{MASTER} 1101: f_{CPU} 1110: f_{CPU} 1111: f_{CPU}
5	CORF	R/W	Clock Output Ready Flag 0: Clock output ready 1: Clock output not ready
6	COBF	R/W	Clock Output Busy Flag 0: The clock source selected by clock output is idle 1: The clock source selected by clock output is busy
31:7	Reserved		

6.5.10 APB clock enable register 2 (RCM_APBEN2)

Offset address: 0x28

Reset value: 0x0000 00FF

Field	Name	R/W	Description
1:0	Reserved		
2	WUPTCEN	R/W	Wakeup TMR Clock Enable 0: Disable 1: Enable
3	ADCCEN	R/W	ADC Clock Enable 0: Disable 1: Enable
31:4	Reserved		

6.5.11 Internal high-speed clock adjustment register (RCM_HIRCTRIM)

Offset address: 0x30

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	TRIM	R/W	HIRC adjustment value
31:4	Reserved		

6.5.12 Reset state register (RCM_RSTSTS)

Offset address: 0x38

Reset value: 0x0000 00XX; X means undefined

Access: Access in the form of word, half word and byte, without latency.

Field	Name	R/W	Description
0	WWDTRF	RC_W1	WWDT TMR Reset Flag 0: No reset occurs 1: Reset occurs
1	IWDTRF	RC_W1	IWDT TMR Reset Flag 0: No reset occurs 1: Reset occurs
2	CPURF	RC_W1	CPU Software Reset Flag 0: No CPU software reset occurs 1: CPU software reset occurs
3	Reserved		
4	EMCRF	RC_W1	EMC Reset Flag 0: No reset occurs 1: Reset occurs
31:5	Reserved		

6.5.13 APB clock enable register 3 (RCM_APBEN3)

Offset address: 0x3C

Reset value: 0x0000 0007

Field	Name	R/W	Description
0	TMR1ACEN	R/W	TMR1A Clock Enable 0: Disable 1: Enable
1	USART2CEN	R/W	USART2 Clock Enable 0: Disable 1: Enable
2	USART3CEN	R/W	USART3 Clock Enable 0: Disable 1: Enable
31:3	Reserved		

7 Nested Vector Interrupt Controller (NVIC)

7.1 Full name and abbreviation description of terms

Table 17 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Non Maskable Interrupt	NMI

7.2 Introduction

The Cortex-M0+ core in the product integrates Nested Vectored Interrupt Controller (NVIC), which is closely coupled with the core, and can handle exceptions and interrupts and power management control efficiently and with low delay. Please see *Cortex-M0+ Technical Reference Manual* for more instructions about NVIC.

7.3 Main characteristics

(1) 23 maskable interrupt channels (excluding 16 Cortex-M0+ interrupt lines)

(2) 4 programmable priority levels (use 2-bit interrupt priority level)

(3) Power management control

(4) Low-delay exception and interrupt processing

(5) Realization of system control register

7.4 Interrupt and exception vector table

Table 18 Interrupt and Exception Vector Table

Name	Vector No.	Priority	Vector address	Description
-	-	-	0x0000_0000	Reserved
RST	-	-3	0x0000_0004	Reset
NMI	-	-2	0x0000_0008	Non-maskable interrupt
Hard Fault	-	-1	0x0000_000C	Various hardware faults
SVCall	-	Can be set	0x0000_002C	System service called by SWI instruction
PendSV	-	Can be set	0x0000_0038	Pending system service
SysTick	-	Can be set	0x0000_003C	System tick timer
-	-	-	0x0000_0040	Reserved

Name	Vector No.	Priority	Vector address	Description
WUPT	1	Can be set	0x0000_0044	Automatic wakeup HALT mode interrupt
CMU	2	Can be set	0x0000_0048	Clock controller
EINTA	3	Can be set	0x0000_004C	Port A external interrupt
EINTB	4	Can be set	0x0000_0050	Port B external interrupt
EINTC	5	Can be set	0x0000_0054	Port C external interrupt
EINTD	6	Can be set	0x0000_0058	Port D external interrupt
-	-	-	0x0000_005C	Reserved
-	-	-	0x0000_0060	Reserved
-	-	-	0x0000_0064	Reserved
SPI	10	Can be set	0x0000_0068	SPI interrupt
TMR1_UT	11	Can be set	0x0000_006C	TMR1 update/overrun/underrun/trigger/brake
TMR1_CC	12	Can be set	0x0000_0070	TMR1 capture/compare
TMR2_UO	13	Can be set	0x0000_0074	TMR2 update/overrun
TMR2_CC	14	Can be set	0x0000_0078	TMR2 capture/compare
-	-	-	0x0000_007C	Reserved
-	-	-	0x0000_0080	Reserved
USART1_TX	17	Can be set	0x0000_0084	USART1 transmit
USART1_RX	18	Can be set	0x0000_0088	USART1 receive
I2C	19	Can be set	0x0000_008C	I2C interrupt
-	-	-	0x0000_0090	Reserved
-	-	-	0x0000_0094	Reserved
ADC	22	Can be set	0x0000_0098	ADC interrupt
TMR4	23	Can be set	0x0000_009C	TMR4 interrupt
FMC	24	Can be set	0x0000_00A0	FLASH interrupt
USART3_TX	25	Can be set	0x0000_00A4	USART3 transmit
USART3_RX	26	Can be set	0x0000_00A8	USART3 receive
USART2_TX	27	Can be set	0x0000_00AC	USART2 transmit
USART2_RX	28	Can be set	0x0000_00B0	USART2 receive
TMR1A_UT	29	Can be set	0x0000_00B4	TMR1A update/overrun/underrun/trigger/brake
TMR1A_CC	30	Can be set	0x0000_00B8	TMR1 capture/compare

8 External Interrupt Controller (EINT)

8.1 Introduction

The external interrupt controller (EINT) manages external interrupts and can generate corresponding interrupt requests to CPU/interrupt controller and wake-up requests to power management.

The EINT supports generating up to 6 interrupt requests, in which each interrupt line as an external interrupt request can be configured independently, each interrupt line has an independent mask, and the external interrupt line can also be triggered independently. In addition, EINT has an NMI interrupt.

8.2 Functional Description

8.2.1 External interrupt

All I/O ports of APM32F003x4x6 MCU series have external interrupt capability. In order to use the external interrupt line, the corresponding I/O port needs to be configured as the input port of interrupt enable. For details, please refer to the description of GPIO register.

PC3 is a non-maskable interrupt. When using NMI interrupt, it is required to remap and configure PC3. Please refer to the option byte chapter for details.

The external interrupt control register 1 (EINT_CTRL1) and external interrupt control register 2 (EINT_CTRL2) control the trigger mode of interrupt.

All interrupts can make the processor exit the standby mode. Only external interrupts and some specific interrupts can make the processor exit the halt mode.

If an internal or external interrupt (e.g. clock interrupt) is generated when WFI/WFE is being executed (provided that the SLEEPDEEP bit of Cortex®-M0+ system control register is 1), the WFI (provided that the SLEEPDEEP bit of Cortex®-M0+ system control register is set to 1) instruction will continue to be executed, but this interrupt will immediately call the wakeup process.

- In such case, MCU is actually awakened from halt mode to run mode. The delay of mode switching is t_{WUH}; see the data manual for details.

8.3 Register address mapping

Table19 Register Address Mapping

Register name	Description	Offset address
EINT_CTRL1	Control register 1	0x00

Register name	Description	Offset address
EINT_CTRL2	Control register 2	0x04
EINT_CLR	Interrupt clear register	0x08

8.4 Register functional description

8.4.1 Control register 1 (EINT_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
1:0	PAIT[1:0]	R/W	Port A Interrupt Triggering Configure 00: Falling edge and low level 01: Rising edge 10: Falling edge 11: Rising edge and falling edge
3:2	PBIT[1:0]	R/W	Port B Interrupt Triggering Configure 00: Falling edge and low level 01: Rising edge 10: Falling edge 11: Rising edge and falling edge
5:4	PCIT[1:0]	R/W	Port C Interrupt Triggering Configure 00: Falling edge and low level 01: Rising edge 10: Falling edge 11: Rising edge and falling edge
7:6	PDIT[1:0]	R/W	Port D Interrupt Triggering Configure 00: Falling edge and low level 01: Rising edge 10: Falling edge 11: Rising edge and falling edge
31:8	Reserved		

8.4.2 Control register 2 (EINT_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
1:0	Reserved		
2	NMIT	R/W	Advanced Interrupt Triggering Configure 0: Falling edge 1: Rising edge Note: This bit is set to 1 by the software and can only be written when the external interrupt on PC3 is disabled.
31:3	Reserved		

8.4.3 Interrupt clear register (EINT_CLR)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	PAIC	R/W	Port A Interrupt Clear Write 1 to this bit and the interrupt flag bit will be cleared
1	PBIC	R/W	Port B Interrupt Clear Write 1 to this bit and the interrupt flag bit will be cleared
2	PCIC	R/W	Port C Interrupt Clear Write 1 to this bit and the interrupt flag bit will be cleared
3	PDIC	R/W	Port D Interrupt Clear Write 1 to this bit and the interrupt flag bit will be cleared
5:4	Reserved		
6	NMIC	R/W	NMI Clear Write 1 to this bit and the interrupt flag bit will be cleared
31:7	Reserved		

9 General-Purpose Input/Output Pin (GPIO)

9.1 Full Name and Abbreviation Description of Terms

Table 20 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
P-channel Metal Oxide Semiconductor	P-MOS
N-channel Metal Oxide Semiconductor	N-MOS

9.2 Main characteristics

(1) Input mode
- Analog input
- Floating input
- Pull-up input

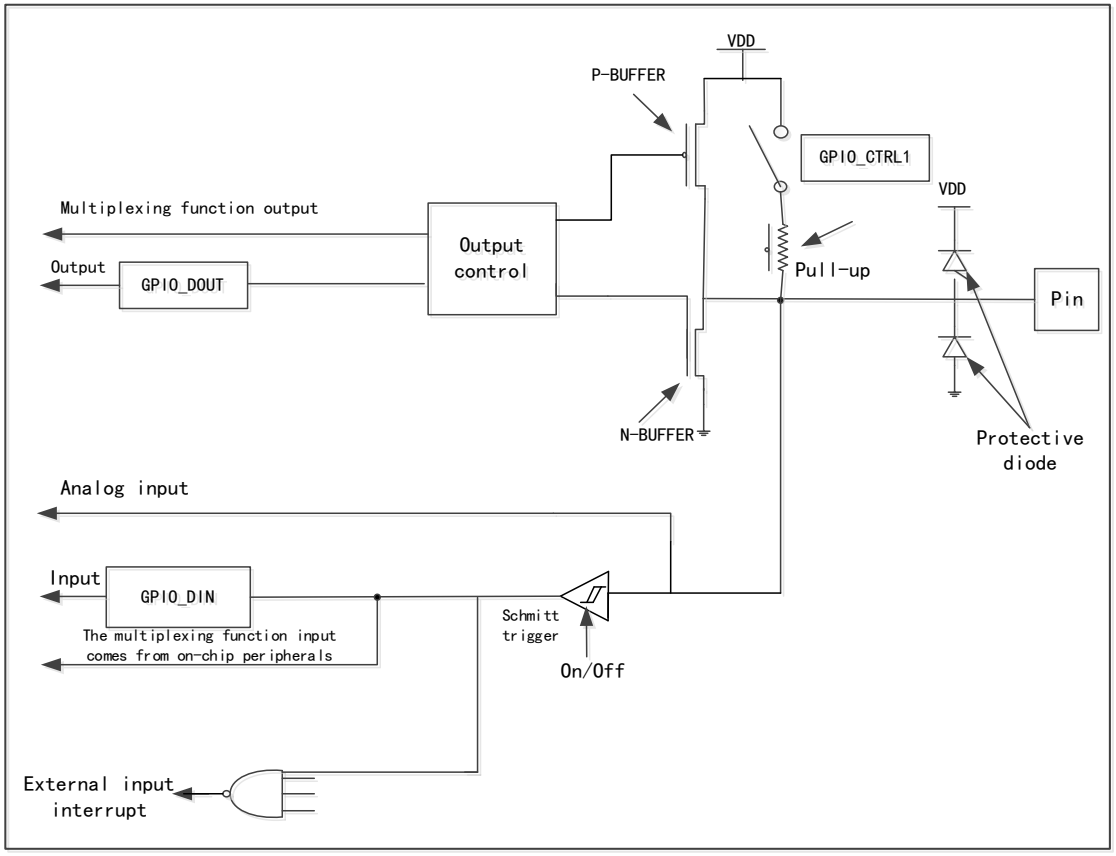
(2) Output mode
- Push-pull output
- Open-drain output
- Configurable maximum output rate

(3) Multiplexing function

(4) GPIO can be used as external interrupt/wakeup line

9.3 Structure block diagram

Figure 10 GPIO Structure Block Diagram



9.4 Functional Description

9.4.1 Input mode

The input mode can be configured as pull-up input and floating input.

9.4.1.1 Multiplexing function input

Some I/O ports have multiplexing function. These functions shall be enabled by configuring the option byte. For details, see the option byte chapter.

For the multiplexed input function, the user shall set I/O port as floating input or pull-up input by configuring GPIOx_MODE and GPIOx_CTRL1 registers.

9.4.1.2 Interrupt function

When I/O pin is in input mode, I/O can be configured as external input interrupt mode by configuring GPIOx_CTRL2 register. At this time, a signal edge or low level on the I/O pin will generate an interrupt request. By configuring EINT_CTRL2 register, select the interrupt trigger mode as rising edge trigger or falling edge trigger.

9.4.1.3 Analog input mode

ADC peripherals can select part of I/O as analog input channel. For analog input mode, GPIOx_MODE, GPIOx_CTRL1 and GPIOx_CTRL2 registers can be configured to set I/O as floating input and disable external input interrupt, and ADC_STD register can be configured to disable the input of Schmitt trigger.

9.4.2 Output mode

The output mode can be configured as push-pull output and open-drain output.

9.4.2.1 Multiplexing function output

When the multiplexing function of the output is enabled, the corresponding peripheral module control output replaces the output of the port data output register.

The peripheral itself and the control register 1 (GPIOx_CTRL1) can set the multiplexing output as pull-up or open-drain output.

9.4.2.2 Speed configuration

By configuring GPIOx_CTRL2 register, select the output speed to be up to 2MHz or 10MHz.

9.4.3 IO state after reset

After reset, all pins are in floating input mode except debug interfaces PD1 and PD2. After reset, the debug pins PD1 and PD2 are configured with multiplexing function, and, PD1 is pull-up mode. When the debugging function is turned off, it is used as a common GPIO pin.

9.5 Register address mapping

Table 21 Register Address Mapping

Register name	Description	Offset address
GPIOx_DOUT	Port output data register	0x00
GPIOx_DIN	Port input data register	0x04
GPIOx_MODE	Port mode register	0x08
GPIOx_CTRL1	Port control register 1	0x0C
GPIOx_CTRL2	Port control register 2	0x10
GPIO_JTAGDIS	JTAG disable register	0x100

9.6 Register functional description

9.6.1 Port output data register (GPIOx_DOUT) (x=A, B, C, D)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DOUTy	R/W	Port OUT Value Configure (y=0…7) If data is written to this register in output mode, a numerical value is obtained, which is applied to the I/O pin via the latch. Reading this register returns the previously latched value. If data is written to this register in input mode, a numerical value is obtained, which is latched to the register (without changing the pin state). The register is cleared after reset. Use the bit read modify write instruction to manipulate a single pin on the data register (without affecting other pins).
31:8	Reserved		

9.6.2 Port input data register (GPIOx_DIN) (x=A, B, C, D)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DINy	R	Port IN Value Configure (y=0…7) 0: Low level 1: High level
31:8	Reserved		

9.6.3 Port mode register (GPIOx_MODE) (x=A, B, C, D)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	MODEy	R/W	Port Mode Configure (y=0…7) 0: Input mode 1: Output mode
31:8	Reserved		

9.6.4 Port control register 1 (GPIOx_CTRL1) (x=A, B, C, D)

Offset address: 0x0C

Reset value: 0x0000 0000 (the reset value of GPIOD_CTRL1 is 0x00000002)

Field	Name	R/W	Description
7:0	CRy	R/W	Port Function Configure (y=0…7) Input mode: 0: Floating input 1: Pull-up input Output mode: 0: Open-drain output 1: Push-pull output

31:8	Reserved

9.6.5 Port control register 2 (GPIOx_CTRL2) (x=A, B, C, D)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CRy	R/W	Port Mode Configure (y=0…7) Input mode: 0: Disable external interrupt 1: Enable external interrupt Output mode: 0: The maximum output speed is 2MHz 1: The maximum output speed is 10MHz
31:8	Reserved		

9.6.6 JTAG disable register (GPIO_JTAGDIS)

Offset address: 0x100

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	JTAGDIS	R/W	JTAG Interface Disable 0: Enable JTAG interface; PD1 is SWDIO, and PD2 is SWCLK 1: Disable JTAG interface; PD1 and PD2 both are ordinary IO
31:1	Reserved		

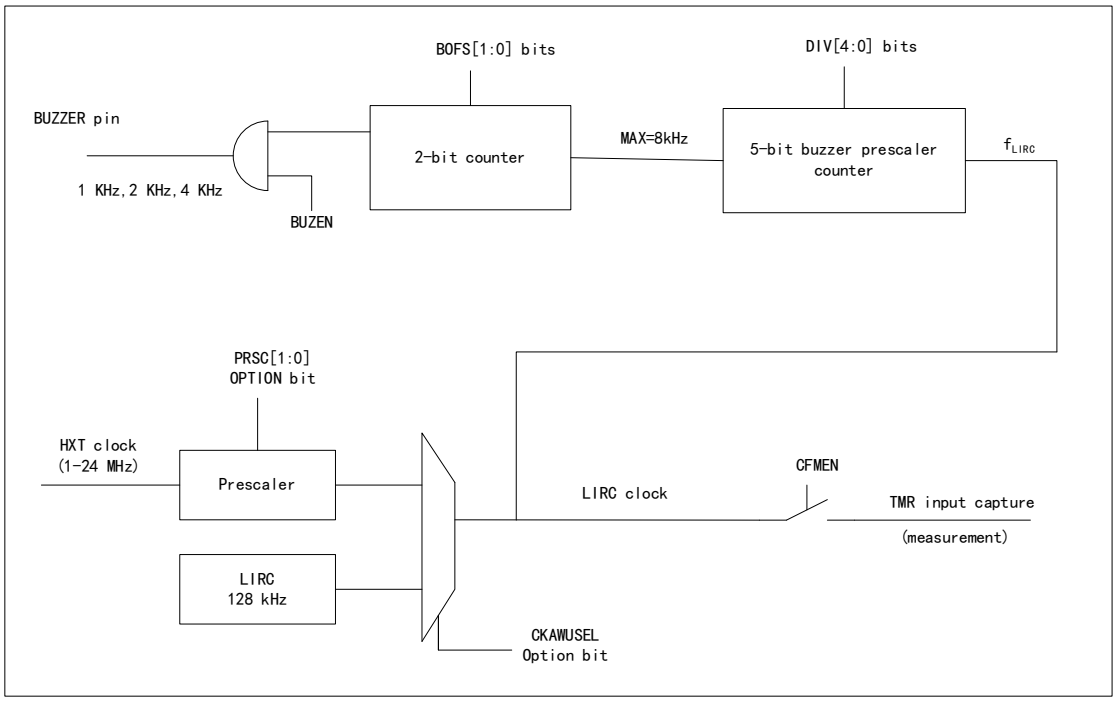
10 Buzzer

10.1 Introduction

When LIRC works at 128KHz, it may generate buzzer signals with frequency of 1KHz, 2KHz or 4KHz.

10.2 Structure block diagram

Figure 11 Structure Function Block Diagram



10.3 Functional Description

To use the buzzer, first calibrate it, then select the frequency to be outputted, and finally enable the clock.

The output frequency formula of buzzer is:

$$\text{Output frequency}=f_{LIRC}/(\text{BOFS x DIV})\ \text{kHz}$$

Wherein, BOFS and DIV are two bits of CSTS register.

10.3.1 Calibration of buzzer

This step can be used to calibrate the clock of LIRC128 kHz to achieve the standard 1 kHz, 2 kHz or 4 kHz frequency output.

The steps are as follows:

(1) Measure the clock frequency of LIRC (please refer to the chapter "LIRC clock frequency detection")

(2) Calculate the value of DIV according to the following method, wherein, A and x are values of integer and fractional parts of $f_{LIRC/8}$ (kHz):

DIV = A-2 when x is less than or equal to A/(1+2*A);

Otherwise, DIV = A-1

(3) Write the value of BUZZERDIV into the DIV[4:0] bit of BUZZER_CSTS.

10.3.2 Use of buzzer

In order to use the buzzer function, the following steps shall be performed in sequence:

(1) Determine the value of DIV[4:0] according to the method described in the chapter "Calibration of buzzer" to calibrate the frequency of LIRC clock;

(2) Select 1 kHz, 2 kHz or 4 kHz output frequency by writing BOFS[1:0] bit of BUZZER_CSTS;

(3) Set BUZEN bit of BUZZER_CSTS to enable the clock source of LIRC;

Note: The prescaler calculator only starts to run when the value of DIV[4:0] is different from the reset value 0x1F.

10.4 Register address mapping

Table 22 Register Address Mapping

Register name	Description	Offset address
BUZZER_CSTS	Control/State register	0x00

10.5 Register functional description

10.5.1 Control/State register (BUZZER_CSTS)

Offset address: 0x00

Reset value: 0x0000 001F

Field	Name	R/W	Description
4:0	DIV	R/W	Buzzer Divider Factor 00000: The factor is 2 00001: The factor is 3 …… 11110: The factor is 32 11111: Reserved

Field	Name	R/W	Description
5	BUZEN	R/W	Buzzer Enable 0: Disable 1: Enable
7:6	BOFS	R/W	Buzzer Output Frequency Select 00: The frequency is f_{LIRC}/(8x DIV) kHz 01: The frequency is f_{LIRC}/(4x DIV) kHz 1X: The frequency is f_{LIRC}/(2x DIV) kHz
31:8	Reserved		

11 Timer Overview

11.1 Full Name and Abbreviation Description of Terms

Table 23 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Timer	TMR
Update	U
Request	R
Event	EV
Capture	C
Compare	C
Length	LEN

11.2 Timer category and main difference

In this series of products, there are three types of timers: advanced timer, general-purpose timer and basic timer (watchdog timer is described in other chapters).

The advanced timer includes the functions of general-purpose timer and basic timer. The advanced timer has four capture/compare channels, supports timing function, input capture and output compare function, braking and complementary output function, and is a timer that can count up/down.

The function of general-purpose timer is simpler than that of advanced timer. The main differences are the total number of channels, the number of complementary output channel groups and the braking function.

The basic timer is a timer that can only realize timing function and has no external interface.

The main differences of timers included in the products are shown in the table below:

Table 24 Main Differences among Timers Included in the Products

Item	Specific content/Category	Advanced timer	General-purpose timer	Basic timer
Name	—	TMR1/TMR1A	TMR2	TMR4
Time base unit	Counter	16 bits		8 bits
	Prescaler factor	Any integer within 1~65536	Any power of 2 within 1~32768	Any power of 2 within 1~128

Item	Specific content/Category	Advanced timer	General-purpose timer	Basic timer
	Count mode	Up Down Center-aligned	Up	
Channel	Capture/Compare channel	4	3	0
	Complementary output channel	Yes	None	None
	External trigger input	1	0	0
	External braking input	1	0	0
Function	PWM	Yes	Yes	None
	Dead zone insertion	Yes	None	None

Timer term

Table 25 Definitions and Terms of Pins

Name	Description
TMRx_ETR	External trigger signal of Timer x
TMRx_CH1, TMRx_CH2, TMRx_CH3, TMRx_CH4	Channel 1/2/3/4 of Timer x
TMRx_CHyN	Complementary output channel y of Timer x
TMRx_BKIN	Braking signal of Timer x

Table 26 Definitions and Terms of Internal Signals

Name	Description
ETR	TMRx_ETR external trigger signal
ETRF	External trigger filter
ETRP	External trigger prescaler
-	
ITR, ITR0, ITR1	Internal trigger
TRGI	Clock/Trigger/Slave mode controller trigger input
TIF_ED	Timer input filter edge detection
-	
CK_PSC	Prescaler clock
CK_CNT	Counter clock
PSC	Prescaler
CNT	Counter

Name	Description
AUTORLD	Autoload register
-	
TIx, TI1	Timer input
TIxF, TI1F	Timer input filter
TI1_ED	Timer input edge detection
TIxFPx, TI1FP1	Timer input filter polarity
ICx, IC1	Input capture
ICxPS, IC1PS	Input capture prescaler
TRC	Trigger capture
BRK	Braking signal
-	
OCx, OC1	Timer output compare channel
OCxREF, OC1REF	Output compare reference signal
-	
TGI	Trigger interrupt
BI	Braking interrupt
CCxI, CC1I	Capture/Compare interrupt
UEV	Update event
UDIE	Update interrupt flag

12 Advanced Timers (TMR1/TMR1A)

12.1 Introduction

The advanced timers TMR1/TMR1A take the time base unit as the core, and have the functions of input capture, output compare and braking input, and include a 16-bit automatic loading counter. Compared with other timers, the advanced timer supports complementary output, repeat count and programmable dead zone insertion function, and is more suitable for motor control.

12.2 Main characteristics

(1) Time base unit
- Counter: 16-bit counter, count-up, count-down and center-aligned count
- Prescaler: 16-bit programmable prescaler
- Repeat counter: 16-bit repeat counter
- Automatic reloading function

(2) Clock source selection
- Internal clock
- External input
- External trigger
- Internal trigger

(3) Input capture function
- Counting function
- PWM input mode (measurement of pulse width, frequency and duty cycle)
- Encoder interface mode

(4) Output compare function
- PWM output mode
- Forced output mode
- Single-pulse mode
- Complementary output and dead zone insertion

(5) Timing function

(6) Braking function

(7) Master/Slave mode controller of timer
- Timers can be synchronized and cascaded (TMR1A cannot be cascaded)
- Support multiple slave modes and synchronization signals

(8) Interrupt output

- Update event (counter overrun/underrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Capture/Compare event
- Braking signal input event

12.3 Structure block diagram

Table 12 TMR1 Structure Block Diagram

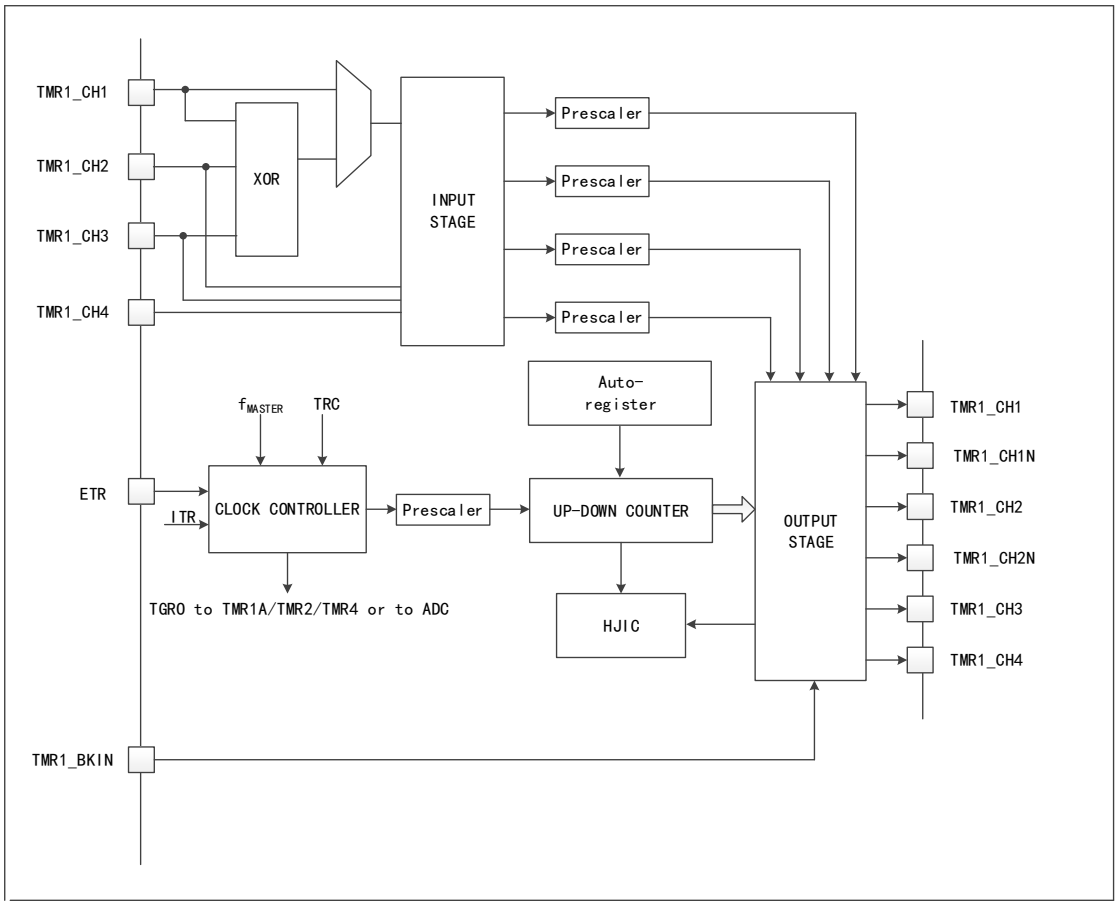
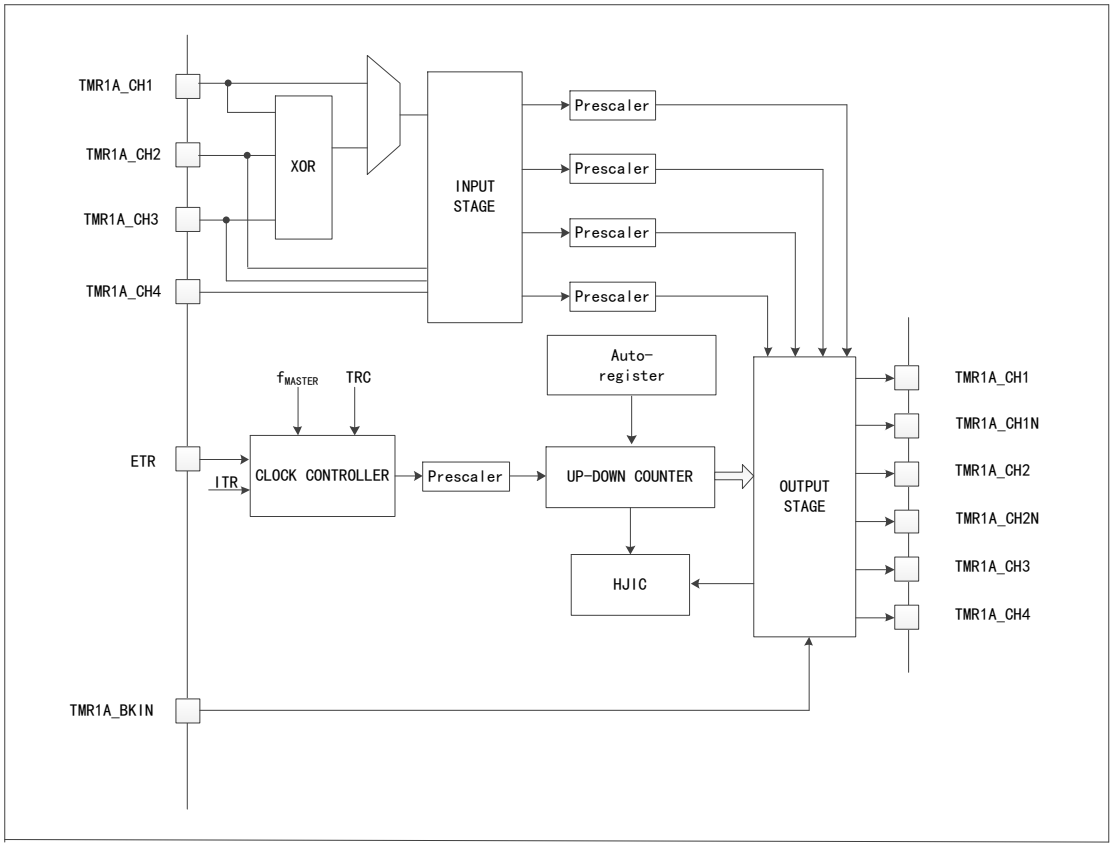


Table 13 TMR1A Structure Block Diagram



12.4 Functional Description

12.4.1 Clock source selection

The advanced timer has four clock sources.

Internal clock

It is TMRx_CLK from RCM, namely the driving clock of the timer; when the slave mode controller is disabled, the clock source CK_PSC of the prescaler is driven by the internal clock CK_INT.

External clock mode 1

The trigger signal generated from the input channel TI1/2/3/4 of the timer after polarity selection and filtering is connected to the slave mode controller to control the work of the counter. Besides, the pulse signal generated by the input of Channel 1 after double-edge detection of the rising edge and the falling edge is logically equal or the future signal is TI1F_ED signal, namely double-edge signal of TIF_ED. Specially the PWM input can only be input by TI1/2.

External clock mode 2

After polarity selection, frequency division and filtering, the signal from external trigger interface (ETR) is connected to the slave mode controller through trigger input selector to control the work of counter.

Internal trigger input

The timer is set to work in slave mode, and the clock source is the output signal of other timers. At this time, the clock source has no filtering, and the synchronization or cascading between timers can be realized. The master mode timer can reset, start, stop or provide clock for the slave mode timer.

12.4.2 Time base unit

The time base unit in the advanced timer contains four registers

- 16-bit counter register (CNT)
- 16-bit auto reload register (AUTORLD)
- 16-bit prescaler register (PSC)
- 8-bit repeat count register (REPCNT)

Counter CNT

There are three counting modes for the counter in the advanced timer

- Count-up mode
- Count-down mode
- Center-aligned mode

Count-up mode

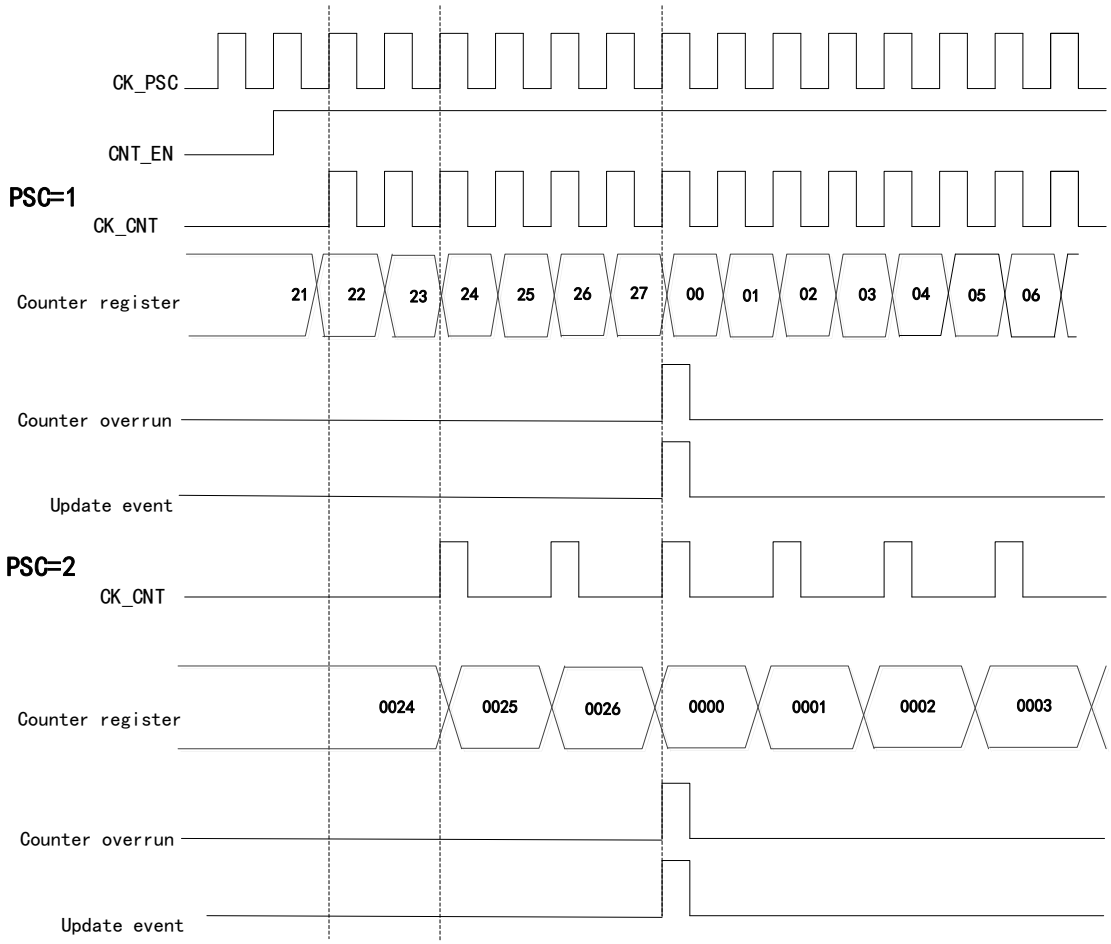
Set to the count-up mode by CNTDIR bit of configuration control register (TMRx_CTRL1).

When the counter is in count-up mode, the counter will count up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMRx_CNT) is equal to the value of the auto reload (TMRx_AUTORLD), the counter will start to count from 0 again, a count-up overrun event will be generated, and the value of the auto reload (TMRx_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the repeat count shadow register, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by NGUE bit of configuration control register TMRx_CTRL1.

The figure below is timing diagram when the division factor is 1 or 2 in count-up mode

Figure 14 Timing Diagram when Division Factor is 1 or 2 in Count-up Mode



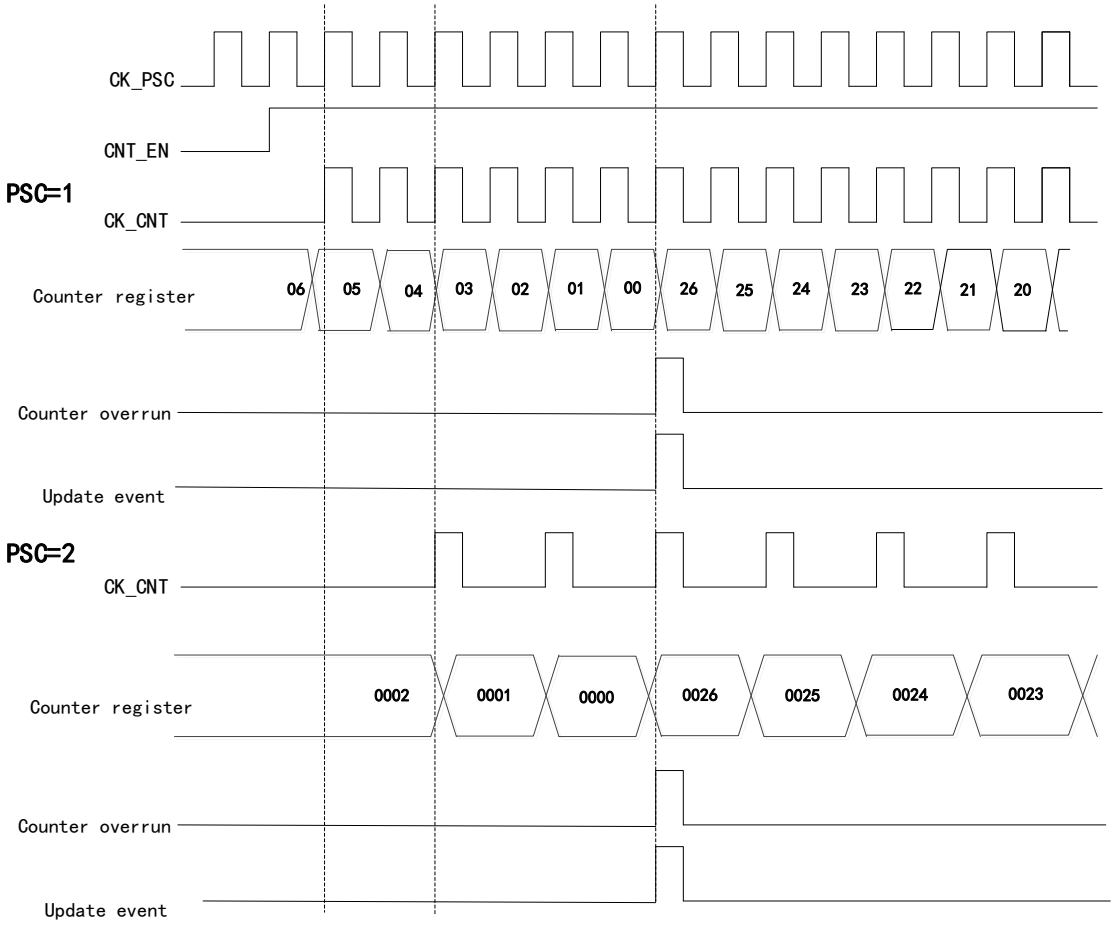
Count-down mode

Set to the count-down mode by CNTDIR bit of configuration control register (TMRx_CTRL1).

When the counter is in count-down mode, it will start to count down from the value of the auto reload (TMRx_AUTORLD); every time a pulse is generated, the counter will decrease by 1 and when it becomes 0, the counter will start to count again from (TMRx_AUTORLD), meanwhile, a count-down overrun event will be generated, and the value of the auto reload (TMRx_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the repeat count shadow register, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by configuring the NGUE bit of the TMRx_CTRL1 register.

Figure 15 Timing Diagram when Division Factor is 1 or 2 in Count-down Mode

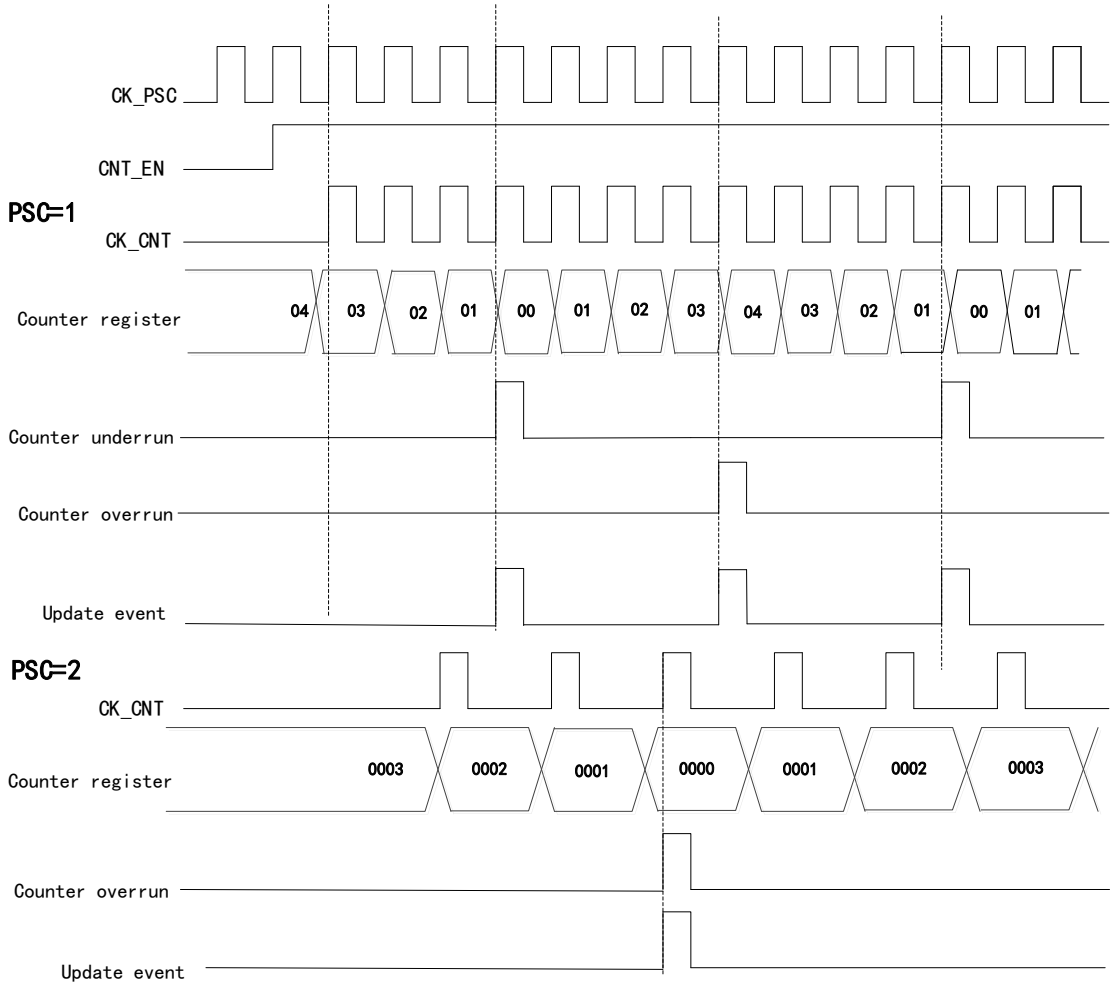


Center-aligned mode

Set to the center-aligned mode by CNTDIR bit of configuration control register (TMRx_CTRL1).

When the counter is in center-aligned mode, the counter counts up from 0 to the value of auto reload (TMRx_AUTORLD), then counts down to 0 from the value of the auto reload (TMRx_AUTORLD), which will repeat; in counting up, when the counter value is (AUTORLD-1), a counter overrun event will be generated; in counting down, when the counter value is 1, a counter underrun event will be generated.

Figure 16 Timing Diagram when Division Factor is 1 or 2 in Center-aligned Mode



Repeat counter REPCNT

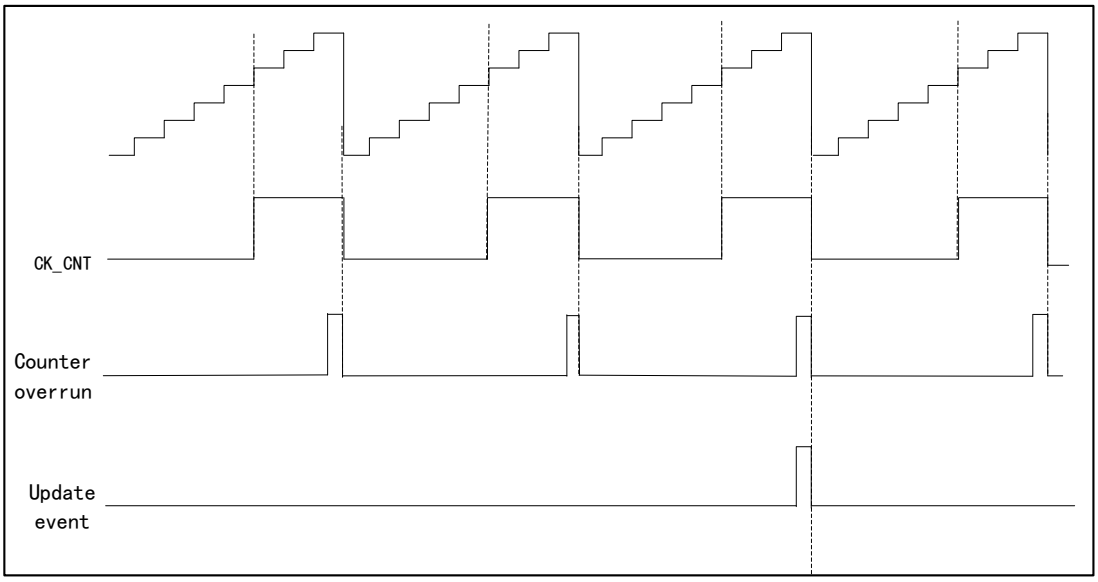
There is no repeat counter REPCNT in the basic/general-purpose timer, which means that when an overrun event or underrun event occurs in the basic/general-purpose timer, an update event will be generated directly; while in the advanced timer, because of the existence of the repeat counter, when an overrun/unerrrun event occurs to the advanced timer, the update event will be generated only when the value of the repeat counter is 0.

For example, if the advanced timer needs to generate an update event when an overrun/underrun event occurs, the value of the repeat counter should be set to 0.

If the repeat counter function is used in the count-up mode, every time the counter counts up to AUTORLD, an overrun event will occur. At this time, the value of the repeat counter will decrease by 1, and an update event will be generated when the value of the repeat counter is 0.

That is, when N+1 (N is the value of repeat counter) overrun/underrun events occur, an update event will be generated.

Figure 17 Timing Diagram when Setting REPCNT=2 in Count-up Mode



Prescaler PSC

The prescaler is 16 bits and programmable, and it can divide the clock frequency of the counter to any value within 1~65536 (controlled by TMRx_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

12.4.3 Input capture

Input capture channel

The advanced timer has four independent capture/compare channels, each of which is surrounded by a capture/compare register.

In the input capture, the measured signal will enter from the external pin T1/2/3/4 of the timer, first pass through the edge detector and input filter, and then into the capture channel. Each capture channel has a corresponding capture register. When the capture occurs, the value of the counter CNT will be latched in the capture register CHxCC. Before entering the capture register, the signal will pass through the prescaler to set how many events to capture at a time.

Input capture application

Input capture is used to capture external events, and can give the time flag to indicate the occurrence time of the event and measure the pulse jump edge events (measure the frequency or pulse width), for example, if the selected edge appears on the input pin, the TMR1_CCx register will capture the current value of the counter and the CCxIFLG bit of the state register TMR1_STS will be set to 1; if CCxIEN=1, an interrupt will be generated.

In capture mode, the timing, frequency, period and duty cycle of a waveform can be measured. In the input capture mode, the edge selection is set to rising edge detection. When the rising edge appears on the capture channel, the first capture occurs, at this time, the value of the counter CNT will be latched in the capture register CHxCC; at the same time, it will enter the capture interrupt, the capture will be recorded in the interrupt service program and the value will be recorded. When the next rising edge is detected, the second capture occurs, the value of counter CNT will be latched in capture register CHxCC again, at this time, it will enter the capture interrupt again, the value of capture register will be read, and the cycle of this pulse signal will be obtained through capture.

12.4.4 Output compare

There are eight modes of output compare: freeze, channel x is valid level when matching, channel x is invalid level when matching, flip, forced to be invalid, forced to be valid, PWM mode 1 and PWM mode 2, which are configured by OCMS bit in TMRx_CHxCCM register and can control the waveform of output signal in output compare mode.

Output compare application

In the output compare mode, the position, polarity, frequency and time of the pulse generated by the timer can be controlled.

When the value of the counter is equal to that of the capture/compare register, the channel output can be set as high level, low level or flip by configuring the OCMS bit in TMRx_CHxCCM register and the CHxCCP bit in the output polarity TMRx_CHCTRL1 register.

12.4.5 PWM output mode

PWM mode is pulse signal that can be adjusted by external output of the timer. The pulse width of the signal is determined by the value of the compare register CCx, and the cycle is determined by the value of the auto reload AUTORLD.

PWM output mode contains PWM mode 1 and PWM mode 2; PWM mode 1 and PWM mode 2 are divided into count-up, count-down and edge alignment counting; in PWM mode 1, if the value of the counter CNT is less than the value of the compare register CCx, the output level will be valid; otherwise, it will be invalid.

Set the timing diagram in PWM mode 1 when CCx=5, AUTORLD=7

Figure 18 Timing Diagram in PWM1 Count-up Mode

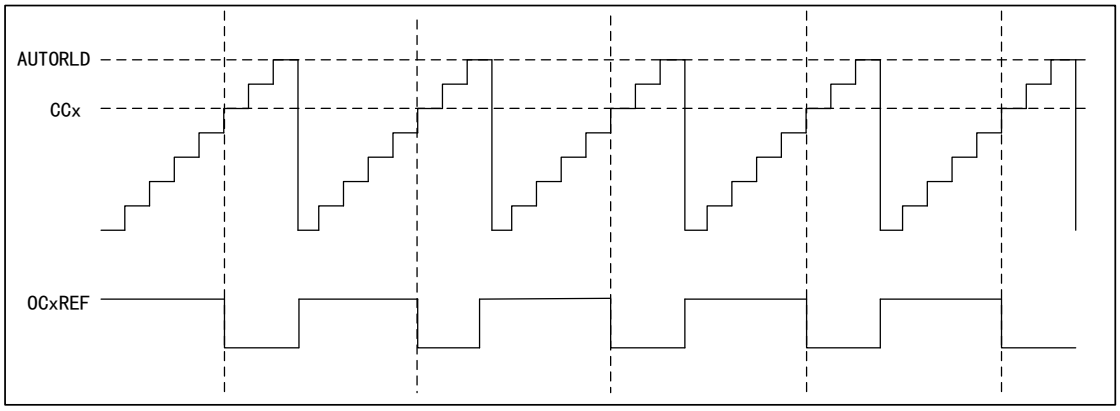


Figure 19 Timing Diagram in PWM1 Count-down Mode

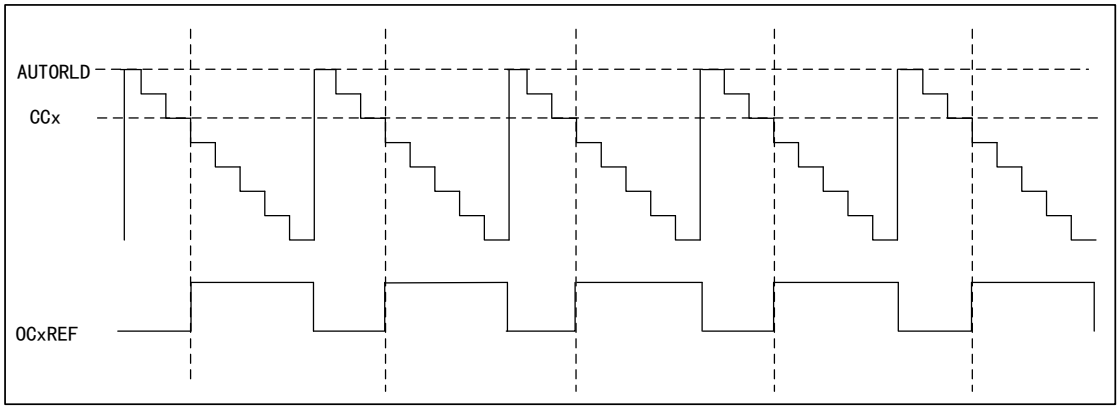
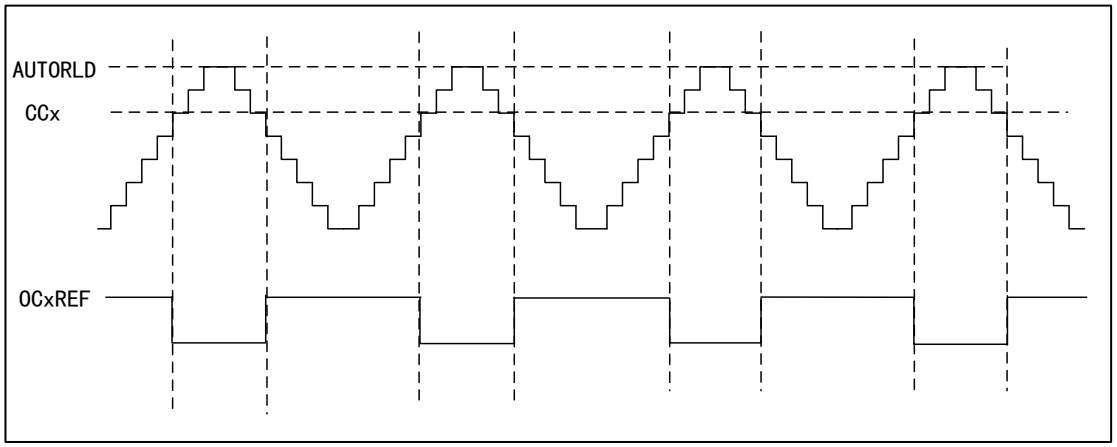


Figure 20 Timing Diagram in PWM1 Center-aligned Mode



In PWM mode 2, if the value of the counter CNT is less than that of the compare register CCx, the output level will be invalid; otherwise, it will be valid.

Set the timing diagram in PWM mode 2 when CCx=5, AUTORLD=7

Figure 21 Timing Diagram in PWM2 Count-up Mode

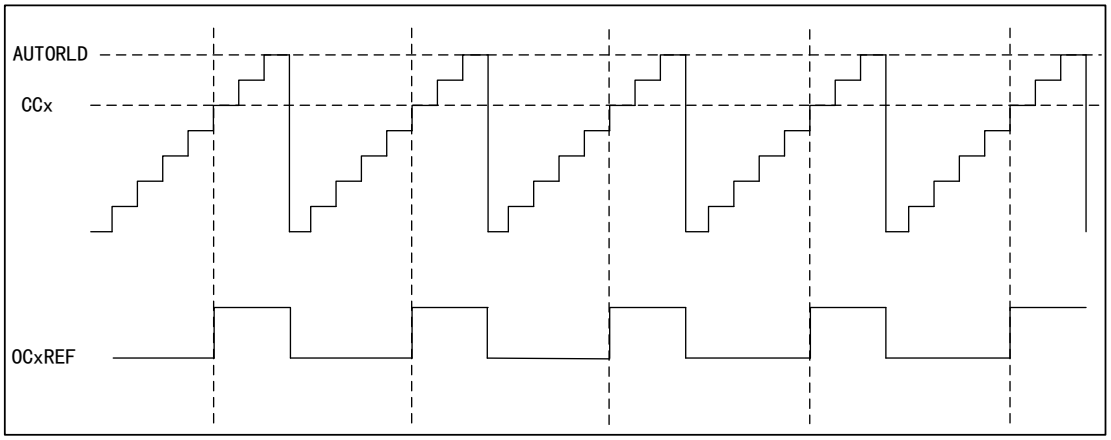


Figure 22 Timing Diagram in PWM2 Count-down Mode

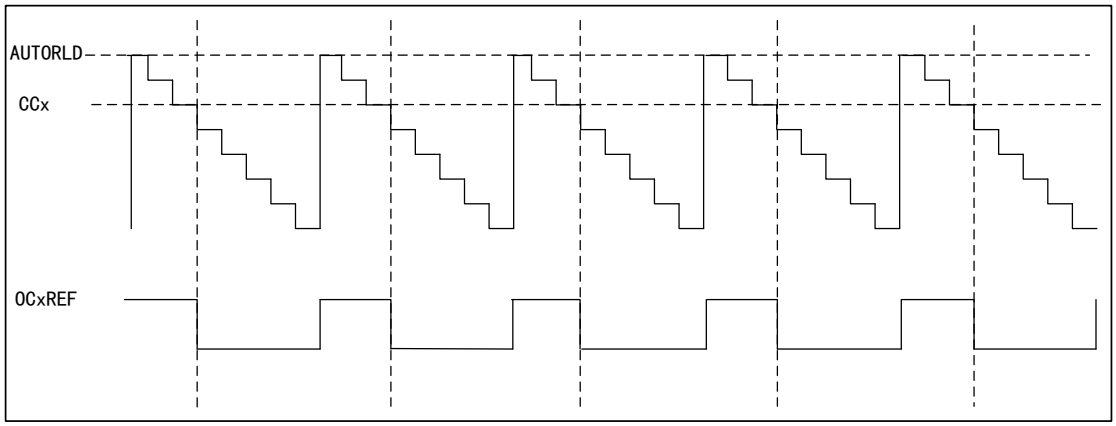
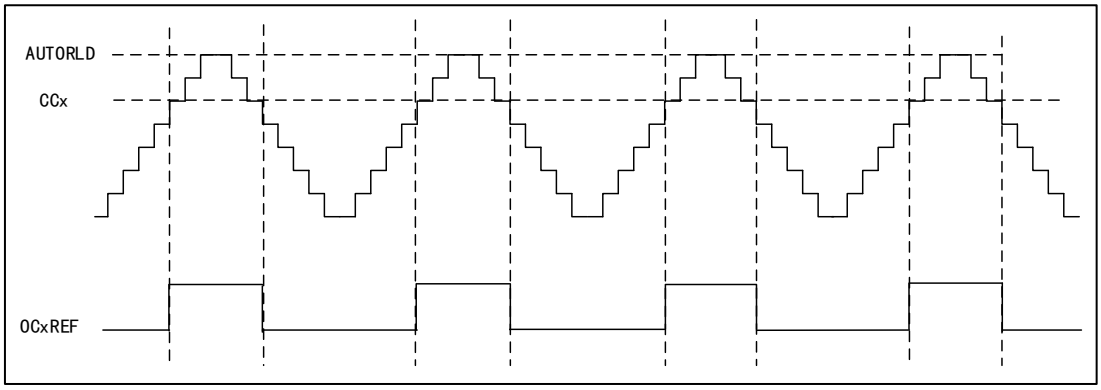


Figure 23 Timing Diagram in PWM2 Center-aligned Mode



12.4.6 PWM input mode

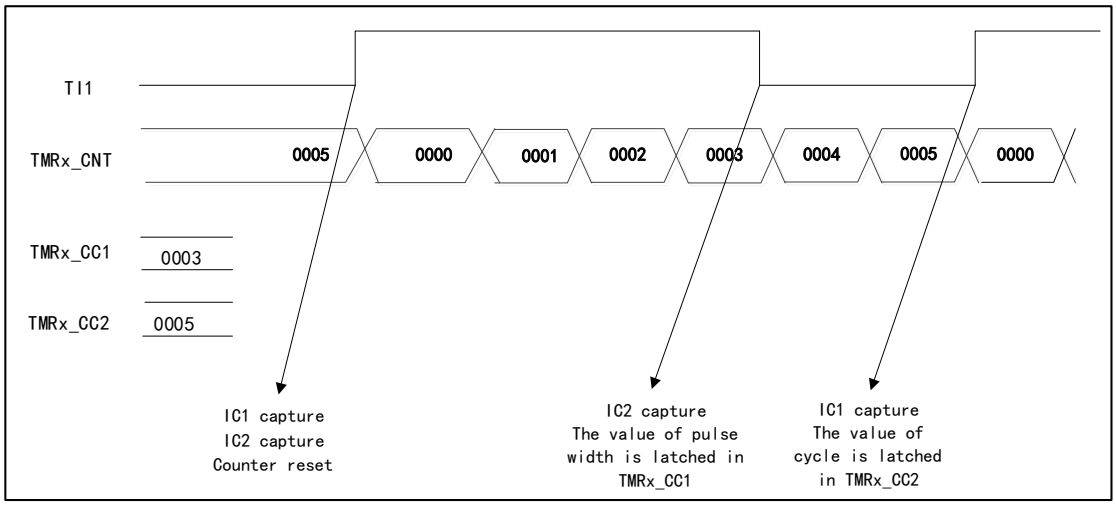
PWM input mode is a particular case of input capture.

In PWM input mode, as only TI1FP1 and TI1FP2 are connected to the slave mode controller, input can be performed only through the channels TMRx_CH1 and TMRx_CH2, which need to occupy the capture registers of CH1 and CH2.

In the PWM input mode, the PWM signal enters from TMRx_CH1, and the signal will be divided into two channels, one can measure the cycle and the other can measure the duty cycle. In the configuration, it is only required to set the polarity of one channel, and the other will be automatically configured with the opposite polarity.

In this mode, the slave mode controller should be configured as the reset mode (SMFC bit of TMRx_SMC register).

Figure 24 Timing Diagram in PWM Input Mode



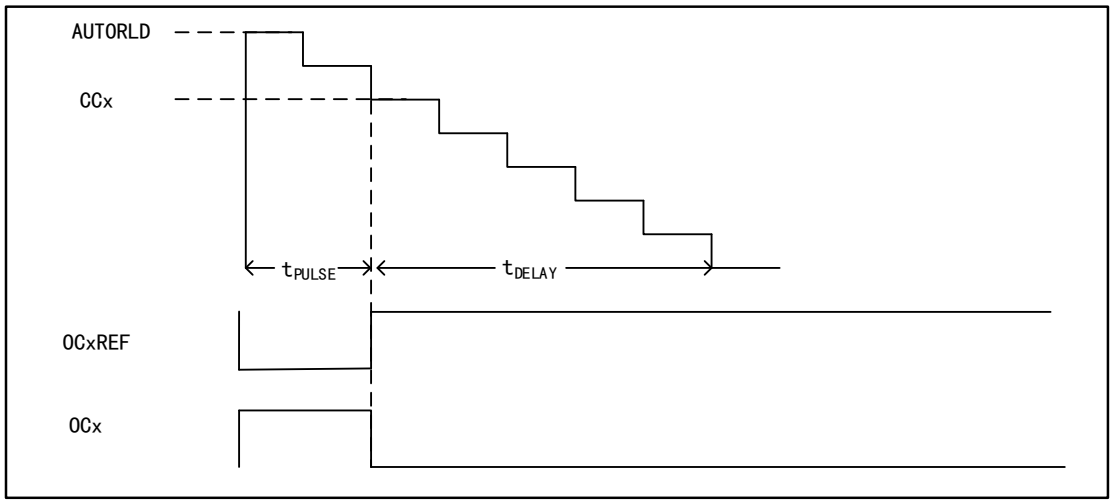
12.4.7 Single-pulse mode

The single-pulse mode is a special case of timer compare output, and is also a special case of PWM output mode.

Set SPMEN bit of TMRx_CTRL1 register, and select the single-pulse mode. After the counter is started, a certain number of pulses will be output before the update event occurs. When an update event occurs, the counter will stop counting, and the subsequent PWM waveform output will no longer be changed.

After a certain controllable delay, a pulse with controllable pulse width is generated in single-pulse mode through the program. The delay time is defined by the value of TMRx_CHxCC register; in the count-up mode, the delay time is CCx and the pulse width is AUTORLD-CCx; in the count-down mode, the delay time is AUTORLD-CCx and the pulse width is CCx.

Figure 25 Timing Diagram in Single-pulse Mode



12.4.8 Impact of the register on output waveform

The following registers will affect the level of the timer output waveform. For details, please refer to "Register Functional Description".

(1) CHxCCEN and CHxOCNEN bits in TMRx_CHCTRL1 register

- CHxOCNEN=0 and CHxCCEN=0: The output is turned off (output disabled, invalid state)
- CHxOCNEN=1 and CHxCCEN=1: The output is turned on (output enabled, normal output)

(2) WOEN bit in TMRx_BRKCTRL register

- WOEN=0: Idle mode
- WOEN=1: Run mode

(3) CHxISO and CHxNISO bits in TMRx_ISO register

- CHxISO=0 and CHxNISO=0: In idle mode (WOEN=0), the output level after the dead zone is 0
- CHxISO=1 and CHxNISO=1: In idle mode (WOEN=0), the output level after the dead zone is 1

(4) RMOS bit in TMRx_BRKCTRL register

- Application environment of RMOS: In corresponding complementary channel and timer run mode (WOEN=1), the timer is not working (CHxCCEN=0, CHxOCNEN=0) or is working (CHxCCEN =1, CHxOCNEN =1)

(5) IMOS bit in TMRx_BRKCTRL register

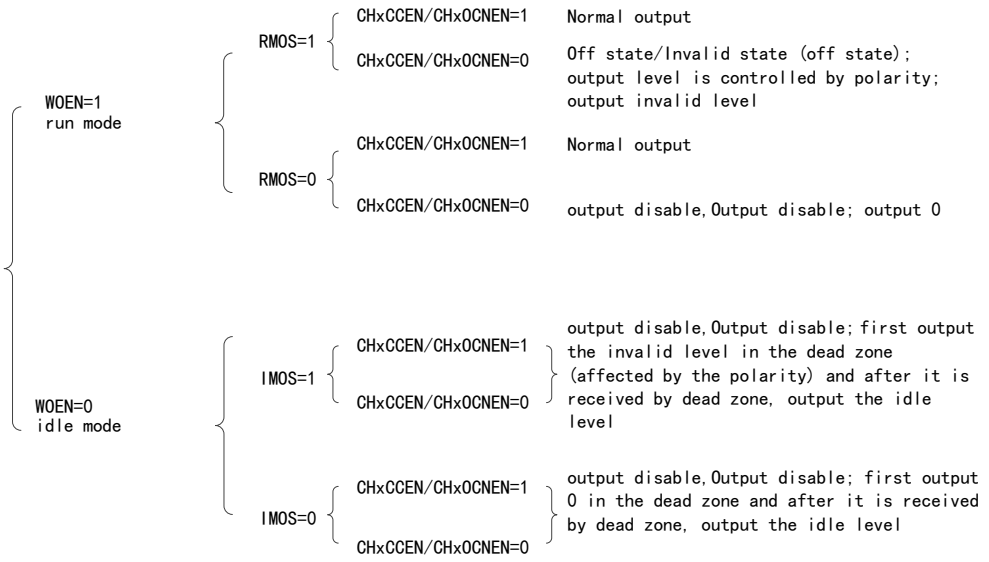
- Application environment of IMOS: In corresponding complementary channel and timer idle mode (WOEN=0), the timer is not working (CHxCCEN=0, CHxOCNEN=0) or is working (CHxCCEN=1, CHxOCNEN=1)

(6) CHxCCP and CHxOCNP bits of TMRx_CHCTRL1 register

- CHxCCP=0 and CHxOCNP=0: Output polarity, high level is valid
  CHxCCP=1 and CHxOCNP=1: Output polarity, the low level is valid

The following figure lists the register structural relationships that affect the output waveform

Figure 26 Register Structural Relationship Affecting Output Waveform



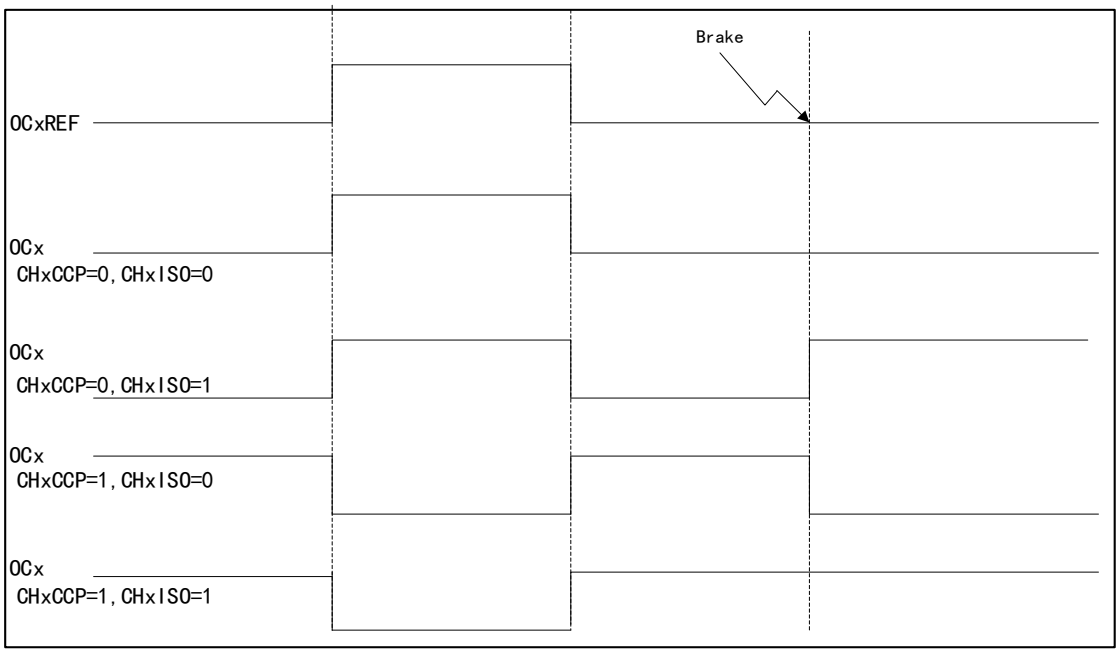
12.4.9 Braking function

The signal source of braking is clock fault event and external input interface.

Besides, the BRKEN bit in TMRx_BRKCTRL register can enable the braking function, and the BRKPOL bit can configure the polarity of braking input signal.

When a braking event occurs, the output pulse signal level can be modified according to the state of the relevant control bit.

Figure 27 Braking Event Timing Diagram

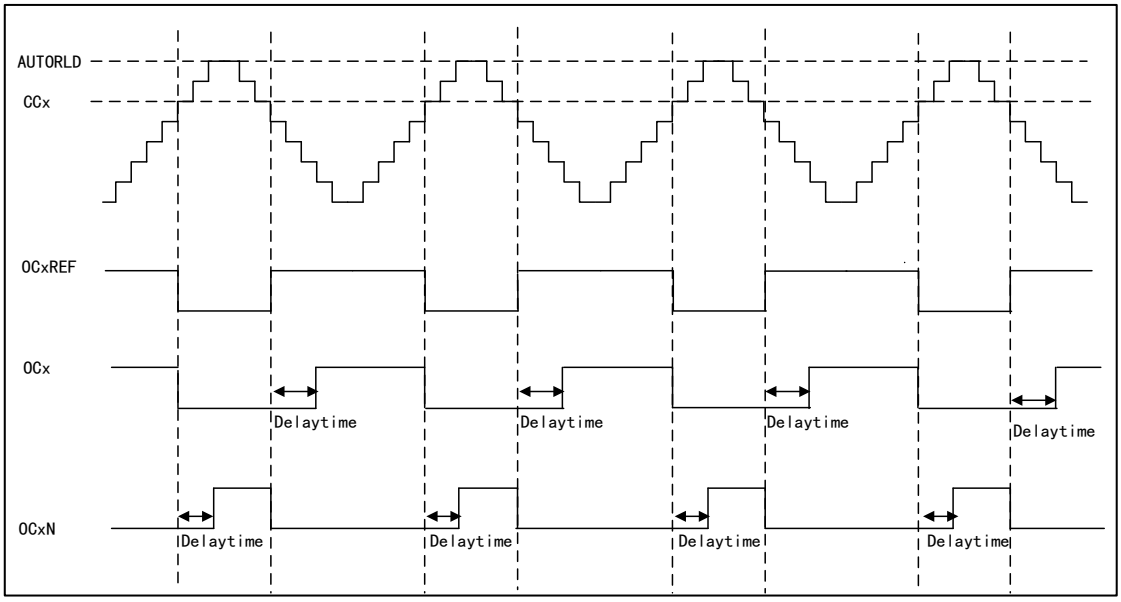


12.4.10 Complementary output and dead zone insertion

TMRx has three groups of complementary output channels. The insertion dead time is used to generate complementary output signals to ensure that the two-way complementary signals of channels will not be valid at the same time. The dead zone time is set according to the output device connected to the timer and its characteristics.

The duration of the dead zone can be controlled by configuring DTS bit of TMRx_DTS register.

Figure 28 Complementary Output with Dead Zone Insertion



12.4.11 Forced output mode

In the forced output mode, the comparison result is ignored, and the corresponding level is directly output according to the configuration instruction.

- MODESEL=00 for TMRx_CHxCCM register, set CCx channel as output
- OCMS=100/101 for TMRx_CHxCCM, set the forced OCxREF signal as invalid/valid state

12.4.12 Encoder interface mode

The encoder interface mode is equivalent to an external clock with direction selection. In the encoder interface mode, the content of the timer can always indicate the position of the encoder.

The selection method of encoder interface is as follows:

- By setting SMFC bit of TMRx_SMC register, the counter can be set to count on the edge of TI1 channel /TI2 channel, or count on the edge of TI1 and TI2 at the same time.
- By setting CH1CCP and CH2CCP bits of TMRx_CHCTRL1 register, the polarity of TI1 and TI2 can be selected.
- By setting ICFC bit of TMRx_CH1CCM register, filtering or not can be selected.

The two input TI1 and TI2 can be used as the interface of incremental encoder. The counter is driven by the effective jump of the signals TI1FP1 and TI2FP2 after filtering and edge selection in TI1 and TI2.

The count pulse and direction signal are generated according to the input signals of TI1 and TI2

- The counter will count up/down according to the jumping sequence of the input signal
- Set CNTDIR of control register TMRx_CTRL1 to be read-only (CNTDIR will be re-calculated due to jumping of any input end)

Table 27 Relationship between Count Direction and Encoder

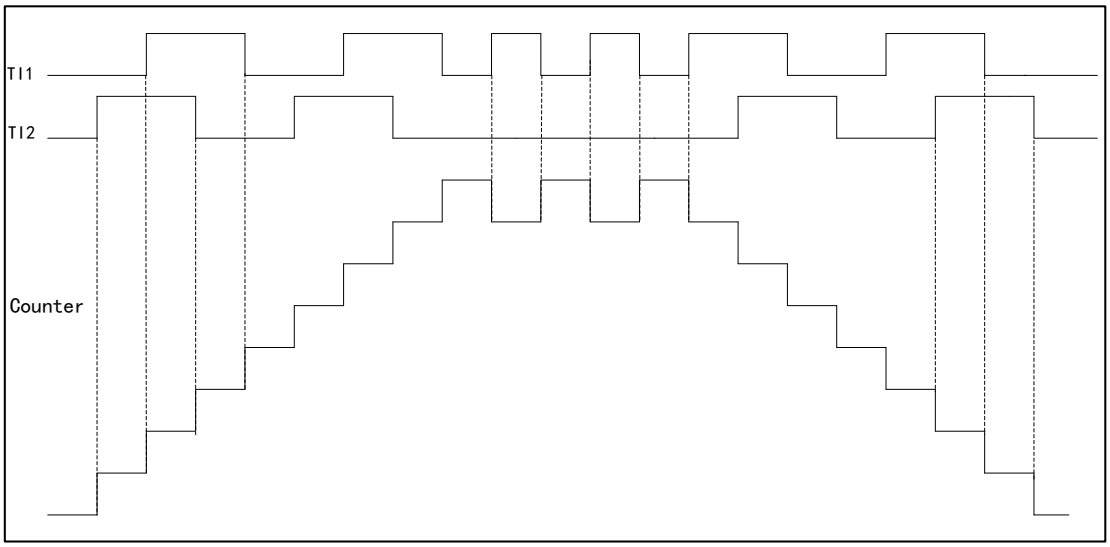
Effective edge		**Count only in TI1**		**Count only in TI2**		**Count in both TI1 and TI2**	
Level of relative signal		High	Low	High	Low	High	Low
TI1FP1	Rising edge	—		Count down	Count up	Count down	Count up
	Falling edge			Count up	Count down	Count up	Count down
TI2FP2	Rising edge	Count up	Count down	—		Count up	Count down
	Falling edge	Count down	Count up			Count down	Count up

The external incremental encoder can be directly connected with MCU, not needing external interface logic, so the comparator is used to convert the differential output of the encoder to digital signal to increase the immunity from noise interference.

Among the following examples:

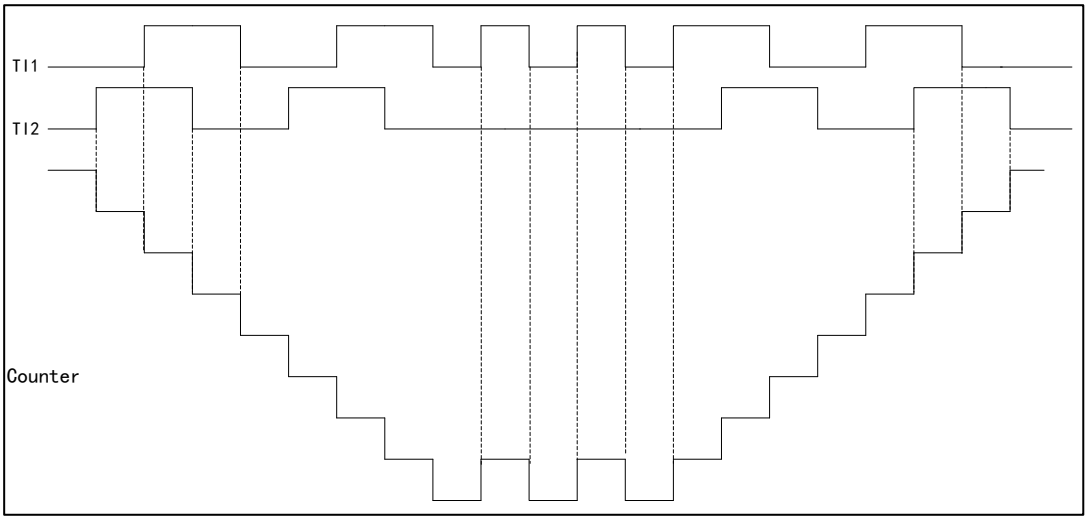
- IC1FP1 is mapped to TI1
- IC2FP2 is mapped to TI2
- Neither IC1FP1 nor IC2FP2 is reverse phase
- The input signal is valid at the rising edge and falling edge
- Enable the counter

Figure 29 Counter Operation Example in Encoder Mode



For example, when TI1 is at low level, and TI2 is in rising edge state, the counter will count up.

Figure 30 Example of Encoder Interface Mode of IC1FP1 Reversed Phase



For example, when TI1 is at low level, and the rising edge of TI2 jumps, the counter will count down.

12.4.13 Slave mode

TMRx timer can synchronize external trigger

- Reset mode
- Gated mode

SMFC bit in TMRx_SMC register can be set to select the mode

SMFC=100 set the reset mode, SMFC=101 set the double-control mode, and SMFC=110 set the single-control mode

In the reset mode, when a trigger input event occurs, the counter and prescaler will be initialized, and the rising edge of the selected trigger input (TRGI) will reinitialize the counter and generate a signal to update the register.

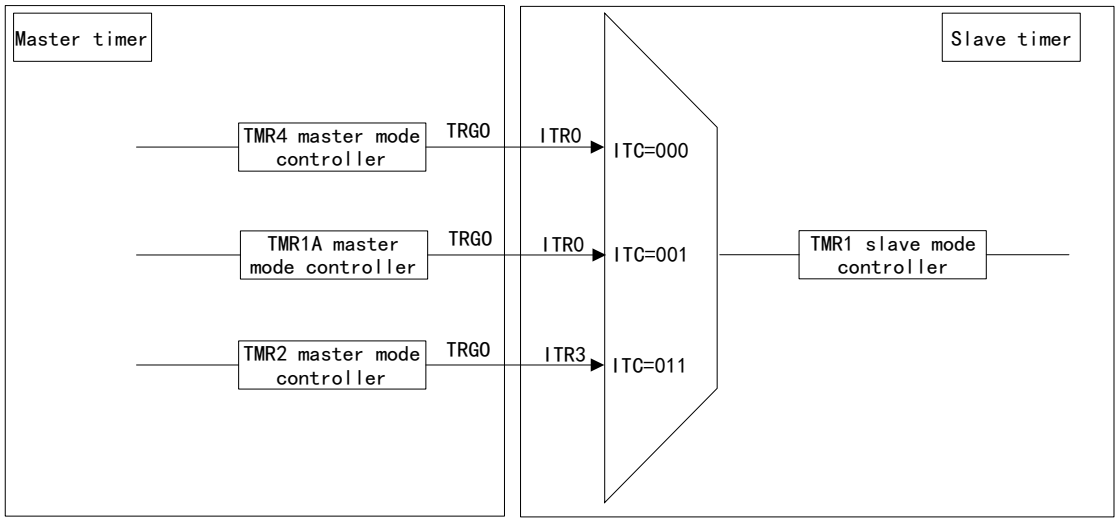
In the gated mode, the enable of the counter depends on the high level of the selected input end. When the trigger input is high, the clock of the counter will be started. Once the trigger input becomes low, the counter will stop (but not be reset). The start and stop of the counter are controlled.

12.4.14 Timer interconnection

Each timer except TMR1A can be connected with each other to realize synchronization or cascading between timers. It is required to configure one timer in master mode and the other timer in slave mode.

When the timer is in master mode, it can reset, start, stop and provide clock source for the counter of the slave mode timer.

Figure 31 Timer 1 Master/Slave Mode Example



When the timers are interconnected:

- A timer can be used as the prescaler of other register
- The other register can be started by the enable signal of a timer
- The other register can be started by the update event of a timer
- The other register can be selected by enabling a timer
- Two timers can be synchronized by an external trigger

12.4.15 Interrupt

The timer can generate an interrupt when an event occurs during operation

- Update event (counter overrun/underrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Capture/Compare event
- Braking signal input event.

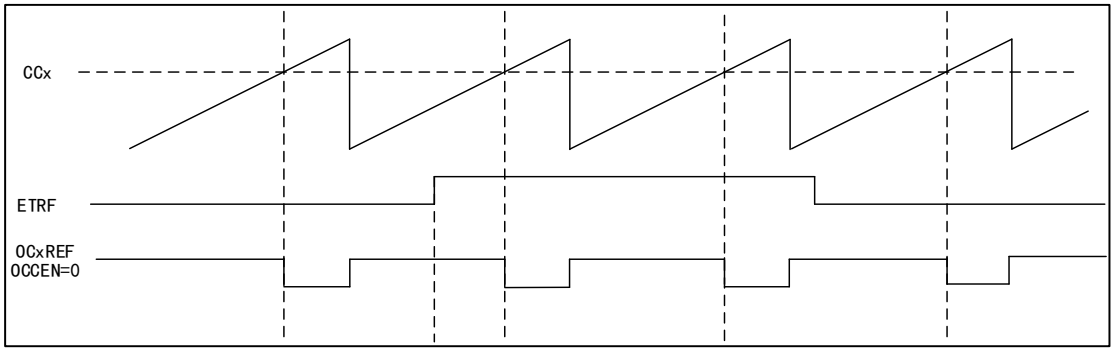
12.4.16 Clear OCxREF signal when an external event occurs

This function is used for output compare and PWM mode.

In one channel, the high level of ETRF input port will reduce the signal of OCxREF to low level, and the OCCEN bit in capture/compare register TMRx_CHxCCM is set to 1, and OCxREF signal will remain low until the next update event occurs.

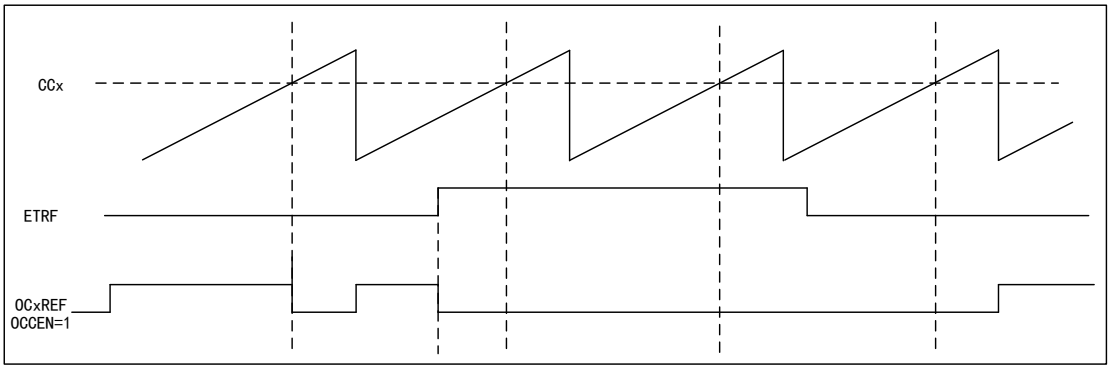
Set TMRx to PWM mode, turn off the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCCEN=0, and the output OCxREF signal is shown in the figure below.

Figure 32 OCxREF Timing Diagram



Set TMRx to PWM mode, turn off the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCCEN=1, and the output OCxREF signal is shown in the figure below.

Figure 33 OCxREF Timing Diagram



12.5 Register address mapping

TMR1 base address: 0x4000_3800

TMR1A base address: 0x4000_1000

Table 28 Register Address Mapping

Register name	Description	Offset address
TMRx_CTRL1	Control register 1	0x00
TMRx_CTRL2	Control register 2	0x04
TMRx_SMC	Slave mode control register	0x08
TMRx_ETC	External trigger control register	0x0C
TMRx_INTCTRL	Interrupt control register	0x10
TMRx_STS1	State register 1	0x14
TMRx_STS2	State register 2	0x18

Register name	Description	Offset address
TMRx_SCEG	Software control event generation register	0x1C
TMRx_CH1CCM	Channel 1 capture/compare mode register	0x20
TMRx_CH2CCM	Channel 2 capture/compare mode register	0x24
TMRx_CH3CCM	Channel 3 capture/compare mode register	0x28
TMRx_CH4CCM	Channel 4 capture/compare mode register	0x2C
TMRx_CHCTRL1	Channel control register 1	0x30
TMRx_CHCTRL2	Channel control register 2	0x34
TMRx_CNT1	Counter register 1	0x38
TMRx_CNT0	Counter register 0	0x3C
TMRx_PSC1	Prescaler register 1	0x40
TMRx_PSC0	Prescaler register 0	0x44
TMRx_AUTORLD1	Auto reload register 1	0x48
TMRx_AUTORLD0	Auto reload register 0	0x4C
TMRx_REPCNT	Repeat count register	0x50
TMRx_CH1CC1	Channel 1 capture/compare register 1	0x54
TMRx_CH1CC0	Channel 1 capture/compare register 0	0x58
TMRx_CH2CC1	Channel 2 capture/compare register 1	0x5C
TMRx_CH2CC0	Channel 2 capture/compare register 0	0x60
TMRx_CH3CC1	Channel 3 capture/compare register 1	0x64
TMRx_CH3CC0	Channel 3 capture/compare register 0	0x68
TMRx_CH4CC1	Channel 4 capture/compare register 1	0x6C
TMRx_CH4CC0	Channel 4 capture/compare register 0	0x70
TMRx_BRKCTRL	Braking control register	0x74
TMRx_DTS	Dead zone register	0x78
TMRx_ISO	Idle state output register	0x7C
TMRx_CHEN	Channel enable register	0x84

12.6 Register functional description

12.6.1 Control register 1 (TMRx_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CNTEN	R/W	Counter Enable 0: Disable 1: Enable When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can write 1 by hardware.
1	NGUE	R/W	No Generated Update Event Update event can cause AUTORLD, PSC and CCx to generate the value of update setting. 0: Update event (UEV) is generated An update event can occur in any of the following situations: The counter overruns/underruns; Set UEG bit; Update generated by slave mode controller. 1: No update event is generated
2	UES	R/W	Update Event Source 0: The counter overruns or underruns Set UEG bit Update generated by slave mode controller 1: The counter overruns or underruns
3	SPMEN	R/W	Single Pulse Mode Enable When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the subsequent output level of the channel will not be changed. 0: Disable 1: Enable
4	CNTDIR	R/W	Counter Direction This bit is read-only when the counter is configured as center-aligned mode or encoder mode. 0: Count up 1: Count down
6:5	CNTMODE	R/W	Center Aligned Mode Select In the center-aligned mode, the counter counts up and down alternately; otherwise, it will only count up or down. Different center-aligned modes affect the timing of setting the output compare interrupt flag bit of the output channel to 1; when the counter is disabled (CNTEN=0), select the center-aligned mode. 00: Edge-aligned mode 01: Center-aligned mode 1 (the output compare interrupt flag bit of output channel is set to 1 when counting down) 10: Center-aligned mode 2 (the output compare interrupt flag bit of output channel is set to 1 when counting up) 11: Center-aligned mode 3 (the output compare interrupt flag bit of output channel is set to 1 when counting up/down)
7	ARBEN	R/W	Auto-reload Preload Enable 0: Disable 1: Enable

Field	Name	R/W	Description
31:8	Reserved		

12.6.2 Control register 2 (TMRx_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CCBEN	R/W	Capture/Compare Preloaded Enable This bit affects the change of CHxCCEN, CHxOCNEN and OCMS values; when the buffer is disabled, program modification will immediately affect the setting of timer; when the prescaler is enabled, it will be only updated after CCUEG is set, which affects the setting of timer; this bit takes effect only on channels with complementary output. 0: Disable 1: Enable
1	Reserved		
2	CCUS	R/W	Capture/compare Control Update Select: It takes effect only when the capture/compare preload is enabled (CCBEN=1), and is valid only for complementary output channel. 0: It can only be updated by setting CCUEG bit 1: It can be updated by setting CCUEG bit or rising edge on TRGI
3	Reserved		
6:4	MMFC	R/W	Master Mode Function Configure The signals of timers working in master mode can be used for TRGO, which affects the work of timers in slave mode and cascaded with the master timer, and the specific impact is related to the configuration of slave mode timer. 000: Reset; the reset signal of master mode timer is used for TRGO 001: Enable; the counter enable signal of master mode timer is used for TRGO 010: Update; the update event of master mode timer is used for TRGO 011: Compare pulses; when the master mode timer captures/compares successfully (CCxCCIF=1), a pulse signal is output for TRGO 100: Compare mode 1; OC1REF is used to trigger TRGO 101: Compare mode 2; OC2REF is used to trigger TRGO 110: Compare mode 3; OC3REF is used to trigger TRGO 111: Compare mode 4; OC4REF is used to trigger TRGO
31:7	Reserved		

12.6.3 Slave mode control register (TMRx_SMC)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	SMFC	R/W	Slave Mode Function Configure 000: Disable the slave mode, the timer can be used as master mode timer to affect the work of slave mode timer; if CTRL1_CNTEN=1, the prescaler is directly driven by the internal clock.

Field	Name	R/W	Description
			001: Encoder mode 1; according to the level of TI1FP1, the counter counts at the edge of TI2FP2. 010: Encoder mode 2; according to the level of TI2FP2, the counter counts at the edge of TI1FP1. 011: Encoder mode 3; according to the input level of the other signal, the counter counts at the edge of TI1FP1 and TI2FP2. 100: Reset mode; the slave mode timer resets the counter after receiving the rising edge signal of TRGI and generates the signal to update the register. 101: Double-control mode 110: Single-control mode 111: External clock mode 1; select the rising edge signal of TRGI as the clock source to drive the counter to work.
3	Reserved		
6:4	ITC	R/W	Input Trigger Configure In order to avoid false edge detection when changing the value of this bit, it must be changed when SMFC=0. 000: Internal trigger ITR0 connects to TMR4 TRGO 001: Internal trigger ITR0 connects to TMR1A TRGO 010: Reserved 011: Internal trigger ITR3 connects to TMR2 TRGO 100: Channel 1 input edge detector TIF_ED 101: Channel 1 post-filtering timer input TI1FP1 110: Channel 2 post-filtering timer input TI2FP2 111: External trigger input (ETRF)
7	MSMEN	R/W	Master/slave Mode Enable 0: Invalid 1: Enable the master/slave mode
31:8	Reserved		

12.6.4 External trigger control register (TMRx_ETC)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	ETFC	R/W	External Trigger Filter Configure 0000: Disable filter, sampled by f_{MASTER} 0001: DIV=1, N=2 0010: DIV=1, N=4 0011: DIV=1, N=8 0100: DIV=2, N=6 0101: DIV=2, N=8 0110: DIV=4, N=6 0111: DIV=4, N=8 1000: DIV=8, N=6 1001: DIV=8, N=8 1010: DIV=16, N=5 1011: DIV=16, N=6

Field	Name	R/W	Description
			1100: DIV=16, N=8 1101: DIV=32, N=5 1110: DIV=32, N=6 1111: DIV=32, N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, and a jump is generated by every N events.
5:4	ETRC	R/W	External Trigger Prescaler Configure The external trigger input signal becomes ETRP after frequency division. The signal frequency of ETRP is at most 1/4 of TMRxCLK frequency; when ETR frequency is too high, the ETRP frequency must be reduced through frequency division. 00: Disable the prescaler 01: ETR signal 2 divided frequency 10: ETR signal 4 divided frequency 11: ETR signal 8 divided frequency
6	ECM2EN	R/W	External Clock Mode2 Enable 0: Disable 1: Enable Setting ECM2EN bit has the same function as selecting external clock mode 1 to connect TRGI to ETRF; slave mode (reset, gating, trigger) can be used at the same time with external clock mode 2, but TRGI cannot be connected to ETRF in such case; when external clock mode 1 and external clock mode 2 are enabled at the same time, the input of external clock is ETRF.
7	ETPC	R/W	External Trigger Polarity Configure This bit decides whether the external trigger is reversed. 0: The external trigger is not reversed, and the high level or rising edge is valid 1: The external trigger is reversed, and the low level or falling edge is valid
31:8	Reserved		

12.6.5 Interrupt control register (TMRx_INTCTRL)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	UDIE	R/W	Update Interrupt Enable 0: Disable 1: Enable
1	CH1CCIE	R/W	Capture/Compare Channel1 Interrupt Enable 0: Disable 1: Enable
2	CH2CCIE	R/W	Capture/Compare Channel2 Interrupt Enable 0: Disable 1: Enable
3	CH3CCIE	R/W	Capture/Compare Channel3 Interrupt Enable 0: Disable 1: Enable

Field	Name	R/W	Description
4	CH4CCIE	R/W	Capture/Compare Channel4 Interrupt Enable 0: Disable 1: Enable
5	CCUIE	R/W	Capture/Compare Update Interrupt Enable 0: Disable 1: Enable
6	TRGIE	R/W	Trigger Interrupt Enable 0: Disable 1: Enable
7	BRKIE	R/W	Break Interrupt Enable 0: Disable 1: Enable
31:8	Reserved		

12.6.6 State register 1 (TMRx_STS1)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	UDIF	R/W	Update Event Interrupt Generate Flag 0: Update event interrupt does not occur 1: Update event interrupt occurs When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared to 0 by software; update events are generated in the following situations: (1) NGUE=0 on TMRx_CTRL1 register, and when the value of the repeat counter overruns/underruns, an update event will be generated; (2) UES=0 and NGUE=0 on TMRx_CTRL1 register, configure UEG=1 on TMRx_SCEG register to generate update event, and the counter needs to be initialized by software; (3) UES=0 and NGUE=0 on TMRx_CTRL1 register, and ab update event will be generated when the counter is initialized by trigger event.
1	CH1CCIF	R/W	Capture/Compare Channel1 Interrupt Flag When the capture/compare channel 1 is configured as output: 0: No matching occurs 1: The value of TMRx_CNT matches the value of TMRx_CH1CC When the capture/compare channel 1 is configured as input: 0: Input capture does not occur 1: Input capture occurs It is set to 1 by hardware when a capture event occurs, and can be cleared to 0 by software or by reading TMRx_CH1CC register.
2	CH2CCIF	R/W	Capture/Compare Channel2 Interrupt Flag Please refer to CH1CCIF bit

Field	Name	R/W	Description
3	CH3CCIF	R/W	Capture/Compare Channel3 Interrupt Flag Please refer to CH1CCIF bit
4	CH4CCIF	R/W	Capture/Compare Channel4 Interrupt Flag Please refer to CH1CCIF bit
5	CCUIF	R/W	Capture/Compare Update Interrupt Flag 0: No capture/compare update interrupt occurs 1: Capture/compare update interrupt occurs When a capture/compare update interrupt occurs, this bit is set to 1 by hardware and cleared to 0 by software.
6	TRGIF	R/W	Trigger Event Interrupt Generate Flag 0: Trigger event interrupt does not occur 1: Trigger event interrupt occurs When a trigger event is generated, this bit is set to 1 by hardware and cleared to 0 by software.
7	BRKIF	R/W	Break Event Interrupt Generate Flag 0: Brake event does not occur 1: Brake event occurs When brake input is valid, this bit is set to 1 by hardware; when brake input is invalid, this bit can be cleared to 0 by software.
31:8	Reserved		

12.6.7 State register 2 (TMRx_STS2)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	Reserved		
1	CH1RCF	R/W	Capture/Compare Channel1 Repetition Capture Flag 0: Repeat capture does not occur 1: Repeat capture occurs The value of the counter is captured in TMRx_CH1CC register, and CH1RCF=1; only when the channel is configured as input capture, can this bit be set to 1 by hardware and cleared to 0 by software.
2	CH2RCF	R/W	Capture/compare Channel2 Repetition Capture Flag Please refer to CH1RCF bit
3	CH3RCF	R/W	Capture/compare Channel3 Repetition Capture Flag Please refer to CH1RCF bit
4	CH4RCF	R/W	Capture/compare Channel4 Repetition Capture Flag Please refer to CH1RCF bit
31:5	Reserved		

12.6.8 Software control event generation register (TMRx_SCEG)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	UEG	W	Update Event Generate 0: Invalid 1: Initialize the counter and generate the update event This bit is set to 1 by software, and cleared to 0 by hardware. Note: When an update event is generated, the counter of the prescaler will be cleared to 0, but the prescaler factor remains unchanged. In the count-down mode, the counter reads the value of TMRx_AUTORLD; in center-aligned mode or count-up mode, the counter will be cleared to 0.
1	CH1CCG	W	Capture/Compare Channel1 Event Generation 0: Invalid 1: Capture/Compare event is generated This bit is set to 1 by software, and cleared to 0 automatically by hardware. If Channel 1 is in output mode: When CH1CCIF=1, if CH1CCIE bit is set, the corresponding interrupt request will be generated. If Channel 1 is in input mode: The value of the capture counter is stored in TMRx_CH1CC register; configure CH1CCIF=1, and if CH1CCIE bit is also set, the corresponding interrupt request will be generated; at this time, if CH1CCIF=1, it is required to configure CH1RCF=1.
2	CH2CCG	W	Capture/Compare Channel2 Event Generation Please refer to CH1CCG bit
3	CH3CCG	W	Capture/Compare Channel3 Event Generation Please refer to CH1CCG bit
4	CH4CCG	W	Capture/Compare Channel4 Event Generation Please refer to CH1CCG bit
5	CCUEG	W	Capture/Compare Control Update Event Generate 0: Invalid 1: Capture/Compare update event is generated This bit is set to 1 by software and cleared to 0 automatically by hardware. Note: CCUEG bit is valid only in complementary output channel.
6	TEG	W	Trigger Event Generate 0: Invalid 1: Trigger event is generated This bit is set to 1 by software and cleared to 0 automatically by hardware.
7	BEG	W	Break Event Generate 0: Invalid 1: Brake event is generated This bit is set to 1 by software and cleared to 0 automatically by hardware.
31:8	Reserved		

12.6.9 Channel 1 capture/compare mode register (TMRx_CH1CCM)

Offset address: 0x20

Reset value: 0x0000 0000

The timer can be configured as input (capture mode) or output (compare mode) by MODESEL bit. The functions of other bits of the register are different in input and output modes, and the functions of the same bit are different in output

mode and input mode. The OCxx in the register describes the function of the channel in the output mode, and the ICxx in the register describes the function of the channel in the input mode.

Output compare mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel1 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is closed (TMRx_CHCTRL1 register CH1CCEN=0).
2	OCFEN	R/W	Output Compare Channel1 Fast Enable 0: Disable 1: Enable This bit is used to improve the response of the capture/compare output to the trigger input event.
3	OCBEN	R/W	Output Compare Channel1 Preload Enable 0: Disable preloading function; write the value of TMRx_CH1CC register through the program, and it will take effect immediately. 1: Enable preloading function; write the value of TMRx_CH1CC register through the program, and it will take effect after an update event is generated. Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. When the preload register is uncertain, PWM mode can be used only in single pulse mode (SPMEN=1); otherwise, the following output compare result is uncertain.
6:4	OCMS	R/W	Output Compare Channel 1 Mode Select 000: Freeze The output compare has no effect on OC1REF 001: The output value is high when matching. When the value of counter CNT matches the value CCx of capture/compare register, OC1REF will be forced to be at high level 010: The output value is low when matching. When the value of the counter matches the value of the capture/compare register, OC1REF will be forced to be at low level 011: Output flaps when matching. When the value of the counter matches the value of the capture/compare register, flap the level of OC1REF 100: The output is forced to be low. Force OC1REF to be at low level 101: The output is forced to be high. Force OC1REF to be at high level 110: PWM mode 1 (set to high when the counter value<output compare value; otherwise, set to low) 111: PWM mode 2 (set to high when the counter value>output compare value; otherwise, set to low) Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. In PWM modes 1 and 2, the OC1REF level changes when the comparison result changes or when the output compare mode changes from freeze mode to PWM mode.
7	OCCEN	R/W	Output Compare Channel1 Clear Enable

Field	Name	R/W	Description
			0: OC1REF is unaffected by ETRF input. 1: When high level of ETRF input is detected, OC1REF=0
31:8	Reserved		

Input capture mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel1 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is closed (TMRx_CHCTRL1 register CH1CCEN=0).
3:2	IC1PSC	R/W	Input Capture Channel1 Perscaler Configure 00: PSC=1 01: PSC=2 10: PSC=4 11: PSC=8 PSC is prescaler factor; capture is triggered once by every PSC events.
7:4	ICFC	R/W	Input Capture Channel1 Filter Configure 0000: Disable filter, sampled by f_{MASTER} 0001: DIV=1, N=2 0010: DIV=1, N=4 0011: DIV=1, N=8 0100: DIV=2, N=6 0101: DIV=2, N=8 0110: DIV=4, N=6 0111: DIV=4, N=8 1000: DIV=8, N=6 1001: DIV=8, N=8 1010: DIV=16, N=5 1011: DIV=16, N=6 1100: DIV=16, N=8 1101: DIV=32, N=5 1110: DIV=32, N=6 1111: DIV=32, N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, indicating that a jump is generated by every N events.
31:8	Reserved		

12.6.10 Channel 2 capture/compare mode register (TMRx_CH2CCM)

Offset address: 0x24

Reset value: 0x0000 0000

Please refer to above CH1CCM register description.

Output compare mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel2 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI2 10: CC2 channel is input, and IC2 is mapped on TI1 11: Reserved Note: This bit can be written only when the channel is closed (TMRx_CHCTRL1 register CH2CCEN=0).
2	OCFEN	R/W	Output Compare Channel2 Fast Enable Please refer to CH1CCM_OCFEN.
3	OCBEN	R/W	Output Compare Channel2 Preload Enable Please refer to CH1CCM_OCBEN.
6:4	OCMS	R/W	Output Compare Channel2 Mode Select Please refer to CH1CCM_OCMS.
7	OCCEN	R/W	Output Compare Channel2 Clear Enable Please refer to CH1CCM_OCCEN.
31:8	Reserved		

Input capture mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel2 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI2 10: CC2 channel is input, and IC2 is mapped on TI1 11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is closed (TMRx_CHCTRL1 register CH2CCEN=0).
3:2	IC2PSC	R/W	Input Capture Channel2 Perscaler Configure Please refer to CH1CCM_IC1PSC.
7:4	ICFC	R/W	Input Capture Channel2 Filter Configure Please refer to CH1CCM_ICFC.
31:8	Reserved		

12.6.11 Channel 3 capture/compare mode register (TMRx_CH3CCM)

Offset address: 0x28

Reset value: 0x0000 0000

Please refer to above CH1CCM register description.

Output compare mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel3 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC3 channel is output 01: CC3 channel is input, and IC3 is mapped on TI3

Field	Name	R/W	Description
			10: CC3 channel is input, and IC3 is mapped on TI4 11: Reserved Note: This bit can be written only when the channel is closed (TMRx_CHCTRL1 register CH3CCEN=0).
2	OCFEN	R/W	Output Compare Channel3 Fast Enable Please refer to CH1CCM_OCFEN.
3	OCBEN	R/W	Output Compare Channel3 Preload Enable Please refer to CH1CCM_OCBEN.
6:4	OCMS	R/W	Output Compare Channel3 Mode Select Please refer to CH1CCM_OCMS.
7	OCCEN	R/W	Output Compare Channel3 Clear Enable Please refer to CH1CCM_OCCEN.
31:8	Reserved		

Input capture mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel3 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC3 channel is output 01: CC3 channel is input, and IC3 is mapped on TI3 10: CC3 channel is input, and IC3 is mapped on TI4 11: Reserved Note: This bit can be written only when the channel is closed (TMRx_CHCTRL1 register CH3CCEN=0).
3:2	IC2PSC	R/W	Input Capture Channel3 Perscaler Configure Please refer to CH1CCM_IC1PSC.
7:4	ICFC	R/W	Input Capture Channel3 Filter Configure Please refer to CH1CCM_ICFC.
31:8	Reserved		

12.6.12 Channel 4 capture/compare mode register (TMRx_CH4CCM)

Offset address: 0x2C

Reset value: 0x0000 0000

Please refer to above CH1CCM register description.

Output compare mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel4 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC4 channel is output 01: CC4 channel is input, and IC4 is mapped on TI3 10: CC4 channel is input, and IC4 is mapped on TI4 11: Reserved Note: This bit can be written only when the channel is closed (TMRx_CHCTRL1 register CH4CCEN=0).
2	OCFEN	R/W	Output Compare Channel4 Fast Enable

Field	Name	R/W	Description
			Please refer to CH1CCM_OCFEN.
3	OCBEN	R/W	Output Compare Channel4 Preload Enable Please refer to CH1CCM_OCBEN.
6:4	OCMS	R/W	Output Compare Channel4 Mode Select Please refer to CH1CCM_OCMS.
7	OCCEN	R/W	Output Compare Channel4 Clear Enable Please refer to CH1CCM_OCCEN.
31:8	Reserved		

Input capture mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel4 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC4 channel is output 01: CC4 channel is input, and IC4 is mapped on TI3 10: CC4 channel is input, and IC4 is mapped on TI4 11: Reserved Note: This bit can be written only when the channel is closed (TMRx_CHCTRL1 register CH3CCEN=0).
3:2	IC2PSC	R/W	Input Capture Channel4 Perscaler Configure Please refer to CH1CCM_IC1PSC.
7:4	ICFC	R/W	Input Capture Channel4 Filter Configure Please refer to CH1CCM_ICFC.
31:8	Reserved		

12.6.13 Channel control register 1 (TMRx_CHCTRL1)

Offset address: 0x30

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CH1CCEN	R/W	Capture/Compare Channel1 Output Enable When CC1 is configured as output: 0: Disable output 1: Enable output When CC1 is configured as input: This bit determines whether the value CNT of the counter can capture and enter TMRx_CH1CC register 0: Disable capture 1: Enable capture
1	CH1CCP	R/W	Capture/Compare Channel1 Output Polarity Configure When CC1 channel is configured as output: 0: OC1 high level is valid 1: OC1 low level is valid When CC1 channel is configured as input: 0: Capture on the high level or rising edge of TI1FP1 1: Capture on the low level or falling edge of TI1FP1

Field	Name	R/W	Description
			When CC1 channel is configured as trigger: 0: Trigger on the high level or rising edge of TI1FP1 1: Trigger on the low level or falling edge of TI1FP1
2	CH1OCNEN	R/W	Capture/Compare Channel1 Complementary Output Enable 0: Disable 1: Enable
3	CH1OCNP	R/W	Capture/Compare Channel1 Complementary Output Polarity 0: OC1N high level is valid 1: OC1N low level is valid. Note: On the complementary output channel, if this bit is preloaded, and CCBEN=1 for TMRx_CTRL2, CH1OCNP can obtain new value from the preload bit only when reversing event is generated. When the protection level is 2 or 3, this bit cannot be modified
4	CH2CCEN	R/W	Capture/Compare Channel2 Output Enable Please refer to CHCTRL1_CH1CCEN
5	CH2CCP	R/W	Capture/Compare Channel2 Output Polarity Configure Please refer to CHCTRL1_CH1CCP
6	CH2OCNEN	R/W	Capture/Compare Channel1 Complementary Output Enable Please refer to CHCTRL1_CH1OCNEN
7	CH2OCNP	R/W	Capture/Compare Channel2 Complementary Output Polarity Configure Please refer to CHCTRL1_CH1OCNP
31:8	Reserved		

Table 29 Control Bits of Complementary Output Channels OCx and OCxN with Braking Function

Control bit					Output state	
WOEN Bit	IMOS Bit	RMOS Bit	CCxE Bit	CCxNE Bit	OCx output state	OCxN output state
1	X	0	0	0	Output disable (disconnected from the timer)	Output disable (disconnected from the timer)
		0	0	1	Output disable (disconnected from the timer)	OCxREF + polarity, OCxN= OCxREF or CCxNP
		0	1	0	OCxREF + polarity, OCx= OCxREF or CCxP	Output disable (disconnected from the timer)
		0	1	1	OCxREF + polarity + dead zone,	OCxREF reverse phase + polarity + dead zone,
		1	0	0	Output disable (disconnected from the timer)	Output disable (disconnected from the timer)

Control bit					Output state	
		1	0	1	Closed (the output is enabled and is at invalid level), OCx=CCxP	OCxREF+ polarity, OCxN= OCxREF or CCxNP
		1	1	0	OCxREF + polarity, OCx= OCxREF or CCxP	Closed (the output is enabled and is at invalid level), OCxN=CCxNP
		1	1	1	OCxREF + polarity + dead zone	OCxREF reverse phase + polarity + dead zone
0	0	X	X	X	Output disable (disconnected from the timer)	
	0					
	0					
	0					
	1				Closed (the output is enabled and is at invalid level); asynchronous: OCx=CCxP, OCxN=CCxNP; then if the clock exist: after one dead zone time, OCx=OISx, OCxN=CHxNISO, assuming both OISx and CHxNISO does not correspond to the valid level of OCx and OCxN.	
	1					
	1					
	1					

Note: The state of external I/O pin connected to the complementary OCx and OCxN channels depends on the state of the OCx and OCxN channels and the GPIO register.

12.6.14 Channel control register 2 (TMRx_CHCTRL2)

Offset address: 0x34

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CH3CCEN	R/W	Capture/Compare Channel3 Output Enable Please refer to CHCTRL1_CH1CCEN
1	CH3CCP	R/W	Capture/Compare Channel3 Output Polarity Configure Please refer to CHCTRL1_CH1CCP
3:2	Reserved		
4	CH4CCEN	R/W	Capture/Compare Channel4 Output Enable Please refer to CHCTRL1_CH1CCEN
5	CH4CCP	R/W	Capture/Compare Channel4 Output Polarity Please refer to CHCTRL1_CH1CCP
31:6	Reserved		

12.6.15 Counter register 1 (TMRx_CNT1)

Offset address: 0x38

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CNT[15:8]	R/W	Counter Value High
31:8	Reserved		

12.6.16 Counter register 0 (TMRx_CNT0)

Offset address: 0x3C

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CNT[7:0]	R/W	Counter Value Low
31:8	Reserved		

12.6.17 Prescaler register 1 (TMRx_PSC1)

Offset address: 0x40

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	PSC[15:8]	R/W	Prescaler Value High Clock frequency of counter (CK_CNT)＝f_{CK_PSC}/(PSC+1)
31:8	Reserved		

12.6.18 Prescaler register 0 (TMRx_PSC0)

Offset address: 0x44

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	PSC[7:0]	R/W	Prescaler Value Low Clock frequency of counter (CK_CNT)＝f_{CK_PSC}/(PSC+1)
31:8	Reserved		

12.6.19 Auto reload register 1 (TMRx_AUTORLD1)

Offset address: 0x48

Reset value: 0x0000 00FF

Field	Name	R/W	Description
7:0	AUTORLD[15:8]	R/W	Auto Reload Value High When the value of auto reload is empty, the counter will not count.
31:8	Reserved		

12.6.20 Auto reload register 0 (TMRx_AUTORLD0)

Offset address: 0x4C

Reset value: 0x0000 00FF

Field	Name	R/W	Description
7:0	AUTORLD[7:0]	R/W	Auto Reload Value Low When the value of auto reload is empty, the counter will not count.
31:8	Reserved		

12.6.21 Repeat count register (TMRx_REPCNT)

Offset address: 0x50

Reset value: 0x0000 00FF

Field	Name	R/W	Description
7:0	REPCNT	R/W	Repetition Counter Value When the count value of the repeat counter is reduced to 0, an update event will be generated, and the counter will start counting again from the REPCNT value; the new value newly written to this register is valid only when an update event occurs in next cycle.
31:8	Reserved		

12.6.22 Channel 1 capture/compare register 1 (TMRx_CH1CC1)

Offset address: 0x54

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[15:8]	R/W	Capture/Compare Channel1 Value High When the capture/compare channel 1 is configured as input mode: It contains the counter value transmitted by the last input capture channel 1 event. When the capture/compare channel 1 is configured as output mode: It contains the current load capture/compare register value Compare the value of the capture and compare channel 1 with the value of the counter to generate the output signal on OC1. When the output compare preload is disabled (OCBEN=0 for TMRx_CH1CCM register), the written value will immediately affect the output compare results; If the output compare preload is enabled (OCBEN=1 for TMRx_CH1CCM register), the written value will affect the output compare result when an update event is generated.
31:8	Reserved		

12.6.23 Channel 1 capture/compare register 0 (TMRx_CH1CC0)

Offset address: 0x58

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[7:0]	R/W	Capture/Compare Channel1 Value Low Please refer to TMRx_CH1CC1
31:8	Reserved		

12.6.24 Channel 2 capture/compare register 1 (TMRx_CH2CC1)

Offset address: 0x5C

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[15:8]	R/W	Capture/Compare Channel2 Value High Please refer to TMRx_CH1CC1
31:8	Reserved		

12.6.25 Channel 2 capture/compare register 0 (TMRx_CH2CC0)

Offset address: 0x60

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[7:0]	R/W	Capture/Compare Channel2 Value Low Please refer to TMRx_CH1CC1
31:8	Reserved		

12.6.26 Channel 3 capture/compare register 1 (TMRx_CH3CC1)

Offset address: 0x64

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[15:8]	R/W	Capture/Compare Channel3 Value High Please refer to TMRx_CH1CC1
31:8	Reserved		

12.6.27 Channel 3 capture/compare register 0 (TMRx_CH3CC0)

Offset address: 0x68

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[7:0]	R/W	Capture/Compare Channel3 Value Low Please refer to TMRx_CH1CC1
31:8	Reserved		

12.6.28 Channel 4 capture/compare register 1 (TMRx_CH4CC1)

Offset address: 0x6c

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[15:8]	R/W	Capture/Compare Channel4 Value High Please refer to TMRx_CH1CC1
31:8	Reserved		

12.6.29 Channel 4 capture/compare register 0 (TMRx_CH4CC0)

Offset address: 0x70

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[7:0]	R/W	Capture/Compare Channel4 Value Low Please refer to TMRx_CH1CC1
31:8	Reserved		

12.6.30 Braking control register (TMRx_BRKCTRL)

Offset address: 0x74

Reset value: 0x0000 0000

Note: According to the lock setting, AOEN, BRKPOL, BRKEN, IMOS, and RMOS bits all can be write-protected, and it is necessary to configure them when writing to TMRx_BRKCTRL register for the first time.

Field	Name	R/W	Description
1:0	PROTCFG	R/W	Lock Write Protection Mode Configure 00: Without lock write protection level; the register can be written directly 01: Lock write protection level 1 It is not allowed to write to BRKEN, BRKPOL and AOEN bits of TMRx_BRKCTRL register, and TMRx_ISO register. 10: Lock write protection level 2 It cannot be written to all bits with protection level 1, CHxCCP bit of TMRx_CHCTRL register, and RMOS and IMOS bits of TMRx_BRKCTRL register. 11: Lock write protection level 3 It is not allowed to write to all bits with protection level 2, and OCMS and OCBEN bits of TMRx_CHxCCM register. Note: After system reset, the lock write protect bit can only be written once.
2	IMOS	R/W	Idle Mode Off-state Configure Idle mode means WOEN=0; closed means CHxCCEN=0; this bit describes the impact of different values for this bit on the output waveform when WOEN=0 and CHxCCEN changes from 0 to 1. 0: Disable OCx/OCxN output 1: First output idle level and then output valid level
3	RMOS	R/W	Run Mode Off-state Configure Run mode means WOEN=1; closed means CHxCCEN=0; this bit describes the impact of different values for this bit on the output waveform when WOEN=1 and CHxCCEN changes from 0 to 1. 0: Disable OCx/OCxN output 1: First output invalid level and then output valid level
4	BRKEN	R/W	Break Function Enable 0: Disable 1: Enable Note: When the protection level is 1, this bit cannot be modified.
5	BRKPOL	R/W	Break Polarity Configure 0: The brake input BRK is valid at low level 1: The brake input BRK is valid at high level Note: When the protection level is 1, this bit cannot be modified. Writing to this bit requires an APB clock delay before it can be used.
6	AOEN	R/W	Automatic Output Enable 0: Disable 1: Enable; when the brake input is invalid, the WOEN bit will be automatically set to 1 at the next update event The WOEN bit can always be set to 1 by software.
7	WOEN	R/W	PWM Main Output Enable 0: Disable the output of OCx and OCxN or force the output of idle state 1: When CHxCCEN and CHxOCNEN bits of the TMRx_CHCTRL1 register are set, turn on OCx and OCxN output

Field	Name	R/W	Description
			When the brake input is valid, it is cleared to 0 by hardware asynchronously. Note: Setting to 1 by software or setting to 1 automatically depends on AOEN bit of the TMRx_BRKCTRL register.

12.6.31 Dead zone register (TMRx_DTS)

Offset address: 0x78

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DTS	R/W	Dead Time Setup DT is the dead zone duration, and the relationship between DT and register DTS is as follows: DTS[7:5]=0xx=>DT=DTS[7:0]×T_{DTS}, T_{DTS}=T_{DTS}; DTS[7:5]=10x=>DT=（64+DTS[5:0]）×T_{DTS}, T_{DTS}=2×T_{DTS}; DTS[7:5]=110=>DT=（32+DTS[4:0]）×T_{DTS}, T_{DTS}=8×T_{DTS}; DTS[7:5]=111=>DT=（32+DTS[4:0]）×T_{DTS}, T_{DTS}=16×T_{DTS}; For example: assuming T_{DTS}=125ns (8MHZ), the dead time setting is as follows: If the step time is 125ns, the dead time can be set from 0 to 15875ns; If the step time is 250ns, the dead time can be set from 16us to 31750ns; If the step time is 1μs, the dead time can be set from 32μs to 63μs; If the step time is 2μs, the dead time can be set from 64μs to 126μs. Note: Once LOCK level (PROTCFG bit in TMRx_BRKCTRL register) is set to 1, 2 or 3, these bits cannot be modified.

12.6.32 Idle state output register (TMRx_ISO)

Offset address: 0x7C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CH1ISO	R/W	OC1 Output Idel State Configure Only the level state after the dead time of OC1 is affected when WOEN=0 and OC1N is realized. 0: OC1=0 1: OC1=1 Note: When PROTCFG bit in TMRx_BRKCTRL register is at the Level 1, 2 or 3, this bit cannot be modified.
1	CH1NISO	R/W	OC1N Output Idle State Configure Only the level state after the dead time of OC1N is affected when WOEN=0 and OC1N is realized. 0: OC1N=0 1: OC1N=1 Note: When PROTCFG bit in TMRx_BRKCTRL register is at the Level 1, 2 or 3, this bit cannot be modified.
2	CH2ISO	R/W	OC2 Output Idel State Configure Please refer to CH1ISO bit.
3	CH2NISO	R/W	OC2N Output Idel State Configure Please refer to CH1NISO bit.

Field	Name	R/W	Description
4	CH3ISO	R/W	OC3 Output Idel State Configure Please refer to CH1ISO bit.
5	Reserved		
6	CH4ISO	R/W	OC4 Output Idel State Configure Please refer to CH1ISO bit.
31:7	Reserved		

12.6.33 Channel enable register (TMRx_CHEN)

Offset address: 0x84

Reset value: 0x0000 0000

Only TMR1A exists in this register, and is used for independent control of channel enable

Field	Name	R/W	Description
0	CH1	R/W	Channel 1 0: Disable 1: Enable
1	CH2	R/W	Channel 2 0: Disable 1: Enable
2	CH3	R/W	Channel 3 0: Disable 1: Enable
3	CH4	R/W	Channel 4 0: Disable 1: Enable
31:4	Reserved		

13 General-purpose Timer (TMR2)

13.1 Introduction

The general-purpose timer takes the time base unit as the core, and has the functions of input capture and output compare, and can be used to measure the pulse width, frequency and duty cycle, and generate the output waveform.

The timers are independent of each other, and they can achieve synchronization and cascading.

13.2 Main characteristics

（1） Time base unit
- Counter: 16-bit counter, count-up count
- Prescaler: 4-bit programmable prescaler
- Automatic reloading function

（2） Clock source selection
- Internal clock
- External input
- External trigger
- Internal trigger

（3） Input function
- Counting function
- PWM input

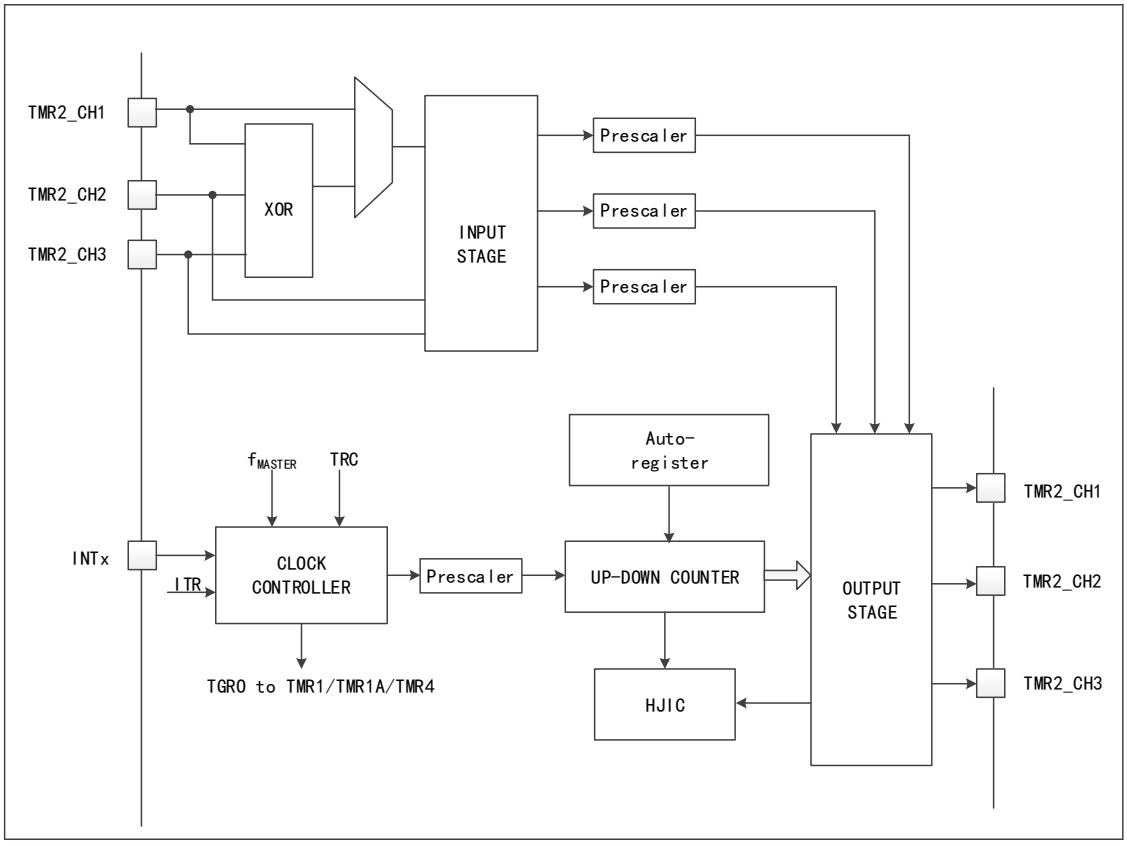
（4） Output function
- PWM output mode
- Forced output mode
- Single-pulse mode

（5） Master/Slave mode controller of timer
- Timers can be synchronized and cascaded
- Support multiple slave modes and synchronization signals

（6） Interrupt request event
- Update event (counter overrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Input capture
- Output compare

13.3 Structure block diagram

Figure 34 General-purpose Timer TMR2 Structure Block Diagram



13.4 Functional Description

13.4.1 Clock source selection

The general-purpose timer has three clock sources

Internal clock

It is TMR2_CLK from RCM, namely the driving clock of the timer; when the slave mode controller is disabled, the clock source CK_PSC of the prescaler is driven by the internal clock CK_INT.

External clock mode 1

The trigger signal generated from the input channel TI1/2/3 of the timer after polarity selection and filtering is connected to the slave mode controller to control the work of the counter. Besides, the pulse signal generated by the input of Channel 1 after double-edge detection of the rising edge and the falling edge is logically equal or the future signal is TI1F_ED signal, namely double-edge signal of TIF_ED. Specially the PWM input can only be input by TI1/2.

Internal trigger input

The timer is set to work in slave mode, and the clock source is the output signal of other timers. At this time, the clock source has no filtering, and the synchronization or cascading between timers can be realized. The master mode timer can reset, start, stop or provide clock for the slave mode timer.

13.4.2 Time base unit

The time base unit in the general-purpose timer contains three registers

- 16-bit counter register (CNT)
- 16-bit auto reload register (AUTORLD)
- 4-bit prescaler register (PSC)

Counter CNT

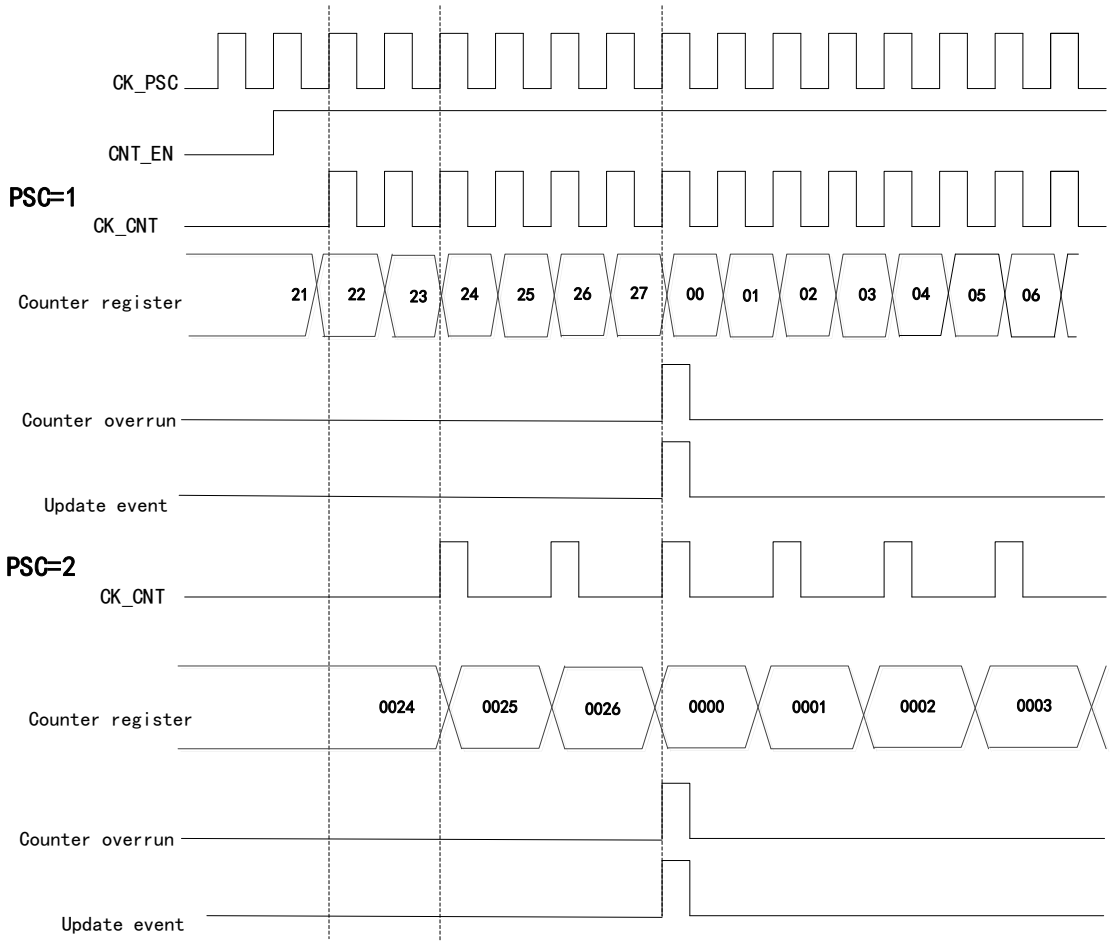
There is only count-up mode for the counter in the general-purpose timer

Count-up mode

The counter counts up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMR2_CNT) is equal to the value of the auto reload (TMR2_AUTORLD), the counter will start to count from 0 again, a counter count-up overrun event will be generated, and the value of the auto reload (TMR2_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by NGUE bit of configuration control register TMR2_CTRL1.

Figure 35 Timing Diagram when Division Factor is 1 or 2 in Count-up Mode



Prescaler PSC

The prescaler is 4 bits and programmable, and it can divide the clock frequency of the counter to any power of 2 between 1 and 32768 (controlled by TMR2_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

13.4.3 Input capture

Input capture channel

The general-purpose timer has three independent capture/compare channels, each of which is surrounded by a capture/compare register.

In the input capture, the measured signal will enter from the external pin T1/2/3 of the timer, first pass through the edge detector and input filter, and then into the capture channel. Each capture channel has a corresponding capture register. When the capture occurs, the value of the counter CNT will be latched in the capture register CHxCC. Before entering the capture register, the signal will pass through the prescaler to set how many events to capture at a time.

Input capture application

Input capture is used to capture external events, and can give the time flag to indicate the occurrence time of the event and measure the pulse jump edge events (measure the frequency or pulse width), for example, if the selected edge appears on the input pin, the TMR2_CHxCC register will capture the current value of the counter and the CCxCCIF bit of the state register TMR2_STS1 will be set to 1; if CH1CCIE=1, an interrupt will be generated.

In capture mode, the timing, frequency, period and duty cycle of a waveform can be measured. In the input capture mode, the edge selection is set to rising edge detection. When the rising edge appears on the capture channel, the first capture occurs, at this time, the value of the counter CNT will be latched in the capture register CHxCC; at the same time, it will enter the capture interrupt, the capture will be recorded in the interrupt service program and the value will be recorded. When the next rising edge is detected, the second capture occurs, the value of counter CNT will be latched in capture register CHxCC again, at this time, it will enter the capture interrupt again, the value of capture register will be read, and the cycle of this pulse signal will be obtained through capture.

13.4.4 Output compare

There are eight modes of output compare: freeze, channel x is valid level when matching, channel x is invalid level when matching, flip, forced to be invalid, forced to be valid, PWM mode 1 and PWM mode 2, which are configured by OCMS bit in TMRx_CHxCCM register and can control the waveform of output signal in output compare mode.

Output compare application

In the output compare mode, the position, polarity, frequency and time of the pulse generated by the timer can be controlled.

When the value of the counter is equal to that of the capture/compare register, the channel output can be set as high level, low level or flip by configuring the OCMS bit in TMR2_CHxCCM register and the CHxCCP bit in the output polarity TMR2_CHCTRL1 register.

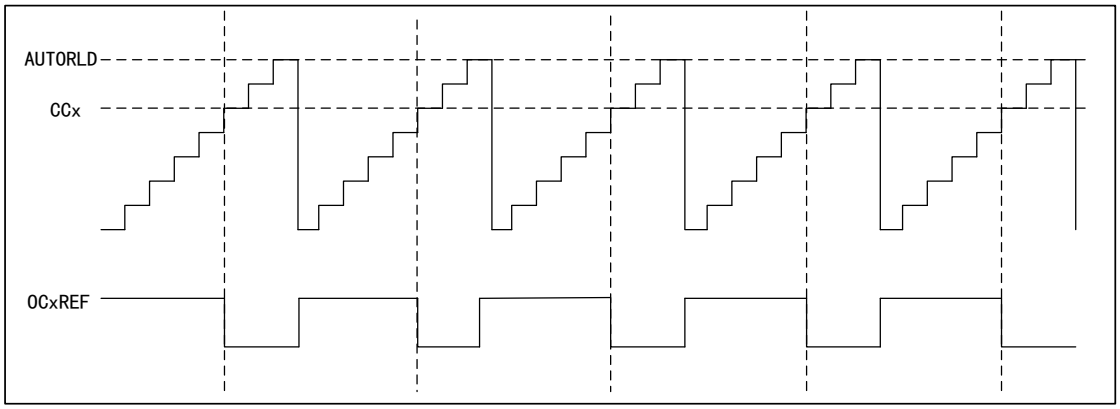
13.4.5 PWM output mode

PWM mode is pulse signal that can be adjusted by external output of the timer. The pulse width of the signal is determined by the value of the compare register CCx, and the cycle is determined by the value of the auto reload AUTORLD.

PWM output mode contains PWM mode 1 and PWM mode 2; PWM mode 1 and PWM mode 2 can only count up; in PWM mode 1, if the value of the counter CNT is less than the value of the compare register CCx, the output level will be valid; otherwise, it will be invalid.

Set the timing diagram in PWM mode 1 when CCx=5, AUTORLD=7

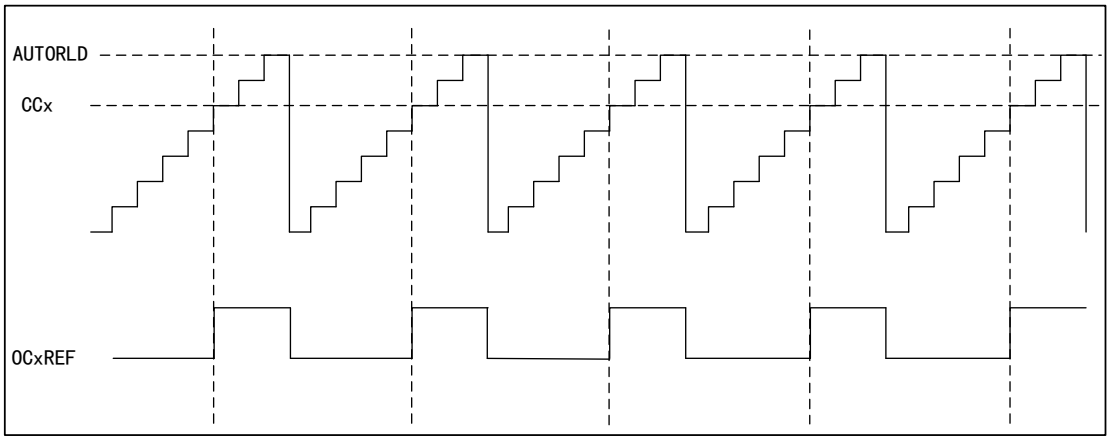
Figure 36 Timing Diagram in PWM1 Count-up Mode



In PWM mode 2, if the value of the counter CNT is less than that of the compare register CCx, the output level will be invalid; otherwise, it will be valid.

Set the timing diagram in PWM mode 2 when CCx=5, AUTORLD=7

Figure 37 Timing Diagram in PWM2 Count-up Mode



13.4.6 PWM input mode

PWM input mode is a particular case of input capture.

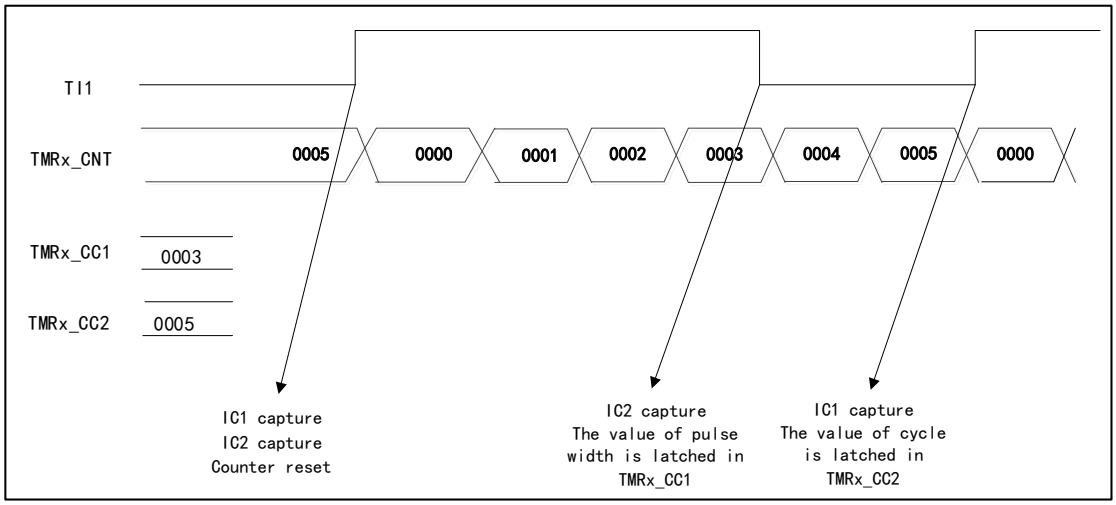
In PWM input mode, as only CH1INFP1 and CH2INFP2 are connected to the slave mode controller, input can be performed only through the channels TMR2_CH1 and TMR2_CH2, which need to occupy the capture registers of CH1 and CH2.

In the PWM input mode, the PWM signal enters from TMR2_CH1, and the signal is divided into two channels, one can measure the cycle and the other can measure the duty cycle. In the configuration, it is only required to set the polarity of one channel, and the other will be automatically configured with the opposite polarity.

In this mode, the slave mode controller should be configured as the reset mode

(SMFC bit of TMR2_SMC register)

Figure 38 Timing Diagram in PWM Input Mode



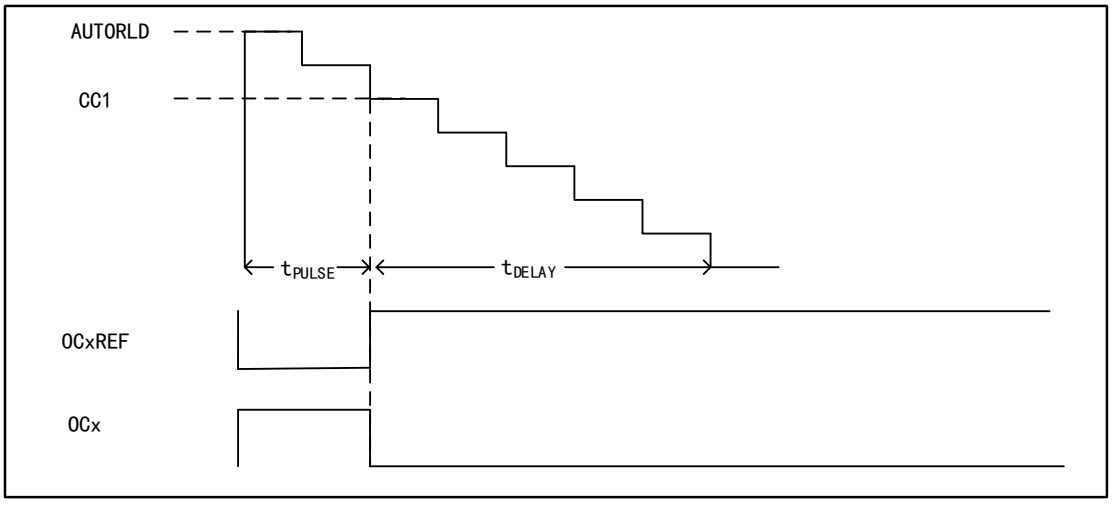
13.4.7 Single-pulse mode

The single-pulse mode is a special case of timer compare output, and is also a special case of PWM output mode.

Set SPMEN bit of TMR2_CTRL1 register, and select the single-pulse mode. After the counter is started, a certain number of pulses will be output before the update event occurs. When an update event occurs, the counter will stop counting, and the subsequent PWM waveform output will no longer be changed.

After a certain controllable delay, a pulse with controllable pulse width is generated in single-pulse mode through the program. The delay time is defined by the value of TMR2_CCx register; in the count-up mode, the delay time is CCx and the pulse width is AUTORLD-CCx; in the count-down mode, the delay time is AUTORLD-CCx and the pulse width is CCx.

Figure 39 Timing Diagram in Single-pulse Mode



13.4.8 Forced output mode

In the forced output mode, the comparison result is ignored, and the corresponding level is directly output according to the configuration instruction.

- MODESEL=00 for TMR2_CHxCCM register, set CCx channel as output
- OCMS=100/101 for TMR2_CHxCCM, set to force OCxREF signal to invalid/valid state

13.4.9 Slave mode

TMR2 timer can synchronize external trigger

- Reset mode
- Gated mode

SMFC bit in TMR2_SMC register can be set to select the mode

SMFC=100 set the reset mode, SMFC=101 set the double-control mode, and SMFC=110 set the single-control mode

In the reset mode, when a trigger input event occurs, the counter and prescaler will be initialized, and the rising edge of the selected trigger input (TRGI) will reinitialize the counter and generate a signal to update the register.

In the gated mode, the enable of the counter depends on the high level of the selected input end. When the trigger input is high, the clock of the counter will be started. Once the trigger input becomes low, the counter will stop (but not be reset). The start and stop of the counter are controlled.

13.4.10 Timer interconnection

See12.4.14 for details.

13.4.11 Interrupt request

The timer can generate an interrupt when an event occurs during operation

- Update event (counter overrun/underrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Capture/Compare event

13.5 Register address mapping

In the following table, all registers of TMR2 are mapped to a 16-bit addressable (address) space.

Table 30 Register Address Mapping

Register name	Description	Offset address
TMRx_CTRL1	Control register 1	0x00
TMRx_CTRL2	Control register 2	0x04

Register name	Description	Offset address
TMRx_SMC	Slave mode control register	0x08
TMRx_INTCTRL	Interrupt control register	0x0C
TMRx_STS1	State register 1	0x10
TMRx_STS2	State register 2	0x14
TMRx_SCEG	Software control event generation register	0x18
TMRx_CH1CCM	Channel 1 capture/compare mode register	0x1C
TMRx_CH2CCM	Channel 2 capture/compare mode register	0x20
TMRx_CH3CCM	Channel 3 capture/compare mode register	0x24
TMRx_CHCTRL1	Channel control register 1	0x28
TMRx_CHCTRL2	Channel control register 2	0x2C
TMRx_CNT1	Counter register 1	0x30
TMRx_ CNT0	Counter register 0	0x34
TMRx_PSC	Prescaler register	0x38
TMRx_AUTORLD1	Auto reload register 1	0x3C
TMRx_AUTORLD0	Auto reload register 0	0x40
TMRx_CH1CC1	Channel 1 capture/compare register 1	0x44
TMRx_CH1CC0	Channel 1 capture/compare register 0	0x48
TMRx_CH2CC1	Channel 2 capture/compare register 1	0x4C
TMRx_CH2CC0	Channel 2 capture/compare register 0	0x50
TMRx_CH3CC1	Channel 3 capture/compare register 1	0x54
TMRx_CH3CC0	Channel 3 capture/compare register 0	0x58

13.6 Register functional description

13.6.1 Control register 1 (TMR2_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CNTEN	R/W	Counter Enable 0: Disable 1: Enable When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can write 1 by hardware.
1	NGUE	R/W	Update Disable Update event can cause AUTORLD, PSC and CCx to generate the value of update setting.

Field	Name	R/W	Description
			0: Enable update event (UEV) An update event can occur in any of the following situations: The counter overruns/underruns; Set UEG bit; Update generated by slave mode controller. 1: Disable update event
2	UES	R/W	Update Request Source Select If the interrupt is enabled, the update event can generate update interrupt request. Different update request sources can be selected through this bit. 0: The counter overruns or underruns Set UEG bit Update generated by slave mode controller 1: The counter overruns or underruns
3	SPMEN	R/W	Single Pulse Mode Enable When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the subsequent output level of the channel will not be changed. 0: Disable 1: Enable
6:4	Reserved		
7	ARBEN	R/W	Auto-reload Preload Enable When the buffer is disabled, the program modification TMR2_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMR2_AUTORLD will modify the values loaded to the counter in the next update event. 0: Disable 1: Enable
31:8	Reserved		

13.6.2 Control register 2 (TMR2_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	Reserved		
6:4	MMFC	R/W	Master Mode Signal Select The signals of timers working in master mode can be used for TRGO, which affects the work of timers in slave mode and cascaded with the master timer, and the specific impact is related to the configuration of slave mode timer. 000: Reset; the reset signal of master mode timer is used for TRGO 001: Enable; the counter enable signal of master mode timer is used for TRGO 010: Update; the update event of master mode timer is used for TRGO 011~111: Reserved
31:7	Reserved		

13.6.3 Slave mode control register (TMR2_SMC)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	SMFC	R/W	Slave Mode Function Select 000: Disable the slave mode, the timer can be used as master mode timer to affect the work of slave mode timer; if CTRL1_CNTEN=1, the prescaler is directly driven by the internal clock. 001~011: Reserved 100: Reset mode; the slave mode timer resets the counter after receiving the rising edge signal of TRGI and generates the signal to update the register. 101: Double-control mode 110: Single-control mode 111: External clock mode 1; select the rising edge signal of TRGI as the clock source to drive the counter to work.
3	Reserved		
6:4	ITC	R/W	Trigger Input Signal Select In order to avoid false edge detection when changing the value of this bit, it must be changed when SMFC=0. 000: Internal trigger ITR0 connects to TMR4 TRGO 001: Internal trigger ITR1 connects to TMR1 TRGO 010: Internal trigger ITR0 connects to TMR1A TRGO 011~111: Reserved
7	MSMEN	R/W	Master/slave Mode Enable 0: Invalid 1: Enable the master/slave mode
31:8	Reserved		

13.6.4 Interrupt control register (TMR2_INTCTRL)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	UDIE	R/W	Update interrupt Enable 0: Disable 1: Enable
1	CH1CCIE	R/W	Capture/Compare Channel1 Interrupt Enable 0: Disable 1: Enable
2	CH2CCIE	R/W	Capture/Compare Channel2 Interrupt Enable 0: Disable 1: Enable
3	CH3CCIE	R/W	Capture/Compare Channel3 Interrupt Enable 0: Disable 1: Enable
5:4	Reserved		

Field	Name	R/W	Description
6	TRGIE	R/W	Trigger Interrupt Enable 0: Disable 1: Enable
31:7	Reserved		

13.6.5 State register (TMR2_STS1)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	UDIF	R/W	Update Event Interrupt Generate Flag 0: Update event interrupt does not occur 1: Update event interrupt occurs When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared to 0 by software.
1	CH1CCIF	R/W	Capture/Compare Channel1 Interrupt Flag When the capture/compare channel 1 is configured as output: 0: No matching occurs 1: The value of TMRx_CNT matches the value of TMRx_CH1CC When the capture/compare channel 1 is configured as input: 0: Input capture does not occur 1: Input capture occurs It is set to 1 by hardware when a capture event occurs, and can be cleared to 0 by software or by reading TMR2_CH1CC register.
2	CH2CCIF	R/W	Capture/Compare Channel2 Interrupt Flag Please refer to CH1CCIF bit
3	CH3CCIF	R/W	Capture/Compare Channel3 Interrupt Flag Please refer to CH1CCIF bit
5:4	Reserved		
6	TRGIF	R/W	Trigger Event Interrupt Generate Flag 0: Trigger event interrupt does not occur 1: Trigger event interrupt occurs When a trigger event is generated, this bit is set to 1 by hardware and cleared to 0 by software.
31:7	Reserved		

13.6.6 State register 2 (TMR2_STS2)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	Reserved		
1	CH1RCF	R/W	Capture/Compare Channel1 Repetition Capture Flag 0: Repeat capture does not occur 1: Repeat capture occurs

Field	Name	R/W	Description
			The value of the counter is captured in TMR2_CH1CC register, and CH1RCF=1; only when the channel is configured as input capture, can this bit be set to 1 by hardware and cleared to 0 by software.
2	CH2RCF	R/W	Capture/compare Channel2 Repetition Capture Flag Please refer to CH1RCF bit
3	CH3RCF	R/W	Capture/compare Channel3 Repetition Capture Flag Please refer to CH1RCF bit
31:4	Reserved		

13.6.7 Software control event generation register (TMR2_SCEG)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	UEG	W	Update Event Generate 0: Invalid 1: Initialize the counter and generate the update event This bit is set to 1 by software, and cleared to 0 by hardware.
1	CH1CCG	W	Capture/Compare Channel1 Event Generation 0: Invalid 1: Capture/Compare event is generated This bit is set to 1 by software and cleared to 0 automatically by hardware. If Channel 1 is in output mode: When CH1CCIF=1, if CH1CCIE bit is set, the corresponding interrupt request will be generated. If Channel 1 is in input mode: The value of the capture counter is stored in TMR2_CH1CC register; configure CH1CCIF=1, and if CH1CCIE bit is also set, the corresponding interrupt request will be generated; at this time, if CH1CCIF=1, it is required to configure CH1RCF=1.
2	CH2CCG	W	Capture/Compare Channel2 Event Generation Please refer to CH1CCG bit
3	CH3CCG	W	Capture/Compare Channel3 Event Generation Please refer to CH1CCG bit
5:4	Reserved		
6	TEG	W	Trigger Event Generate 0: Invalid 1: Trigger event is generated This bit is set to 1 by software and cleared to 0 automatically by hardware.
31:7	Reserved		

13.6.8 Channel 1 capture/compare mode register (TMR2_CH1CCM)

Offset address: 0x1C

Reset value: 0x0000 0000

The timer can be configured as input (capture mode) or output (compare mode) by MODESEL bit. The functions of other bits of the register are different in input

and output modes, and the functions of the same bit are different in output mode and input mode. The OCxx in the register describes the function of the channel in the output mode, and the ICxx in the register describes the function of the channel in the input mode.

Output compare mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel1 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is closed (TMR2_CHCTRL1 register CH1CCEN=0).
2	Reserved		
3	OCBEN	R/W	Output Compare Channel1 Preload Enable 0: Disable preloading function; write the value of TMR2_CH1CC register through the program, and it will take effect immediately. 1: Enable preloading function; write the value of TMR2_CH1CC register through the program, and it will take effect after an update event is generated. Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. When the preload register is uncertain, PWM mode can be used only in single pulse mode (SPMEN=1); otherwise, the following output compare result is uncertain.
6:4	OCMS	R/W	Output Compare Channel 1 Mode Select 000: Freeze The output compare has no effect on OC1REF 001: The output value is high when matching. When the value of counter CNT matches the value CCx of capture/compare register, OC1REF will be forced to be at high level 010: The output value is low when matching. When the value of the counter matches the value of the capture/compare register, OC1REF will be forced to be at low level 011: Output flaps when matching. When the value of the counter matches the value of the capture/compare register, flap the level of OC1REF 100: The output is forced to be low. Force OC1REF to be at low level 101: The output is forced to be high. Force OC1REF to be at high level 110: PWM mode 1 (set to high when the counter value<output compare value; otherwise, set to low) 111: PWM mode 2 (set to high when the counter value>output compare value; otherwise, set to low) Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. In PWM modes 1 and 2, the OC1REF level changes when the comparison result changes or when the output compare mode changes from freeze mode to PWM mode.
31:7	Reserved		

Input capture mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel1 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is closed (TMR2_CHCTRL1 register CH1CCEN=0).
3:2	IC1PSC	R/W	Input Capture Channel1 Perscaler Configure 00: PSC=1 01: PSC=2 10: PSC=4 11: PSC=8 PSC is prescaler factor; capture is triggered once by every PSC events.
7:4	ICFC	R/W	Input Capture Channel1 Filter Configure 0000: Disable filter, sampled by f_{MASTER} 0001: DIV=1, N=2 0010: DIV=1, N=4 0011: DIV=1, N=8 0100: DIV=2, N=6 0101: DIV=2, N=8 0110: DIV=4, N=6 0111: DIV=4, N=8 1000: DIV=8, N=6 1001: DIV=8, N=8 1010: DIV=16, N=5 1011: DIV=16, N=6 1100: DIV=16, N=8 1101: DIV=32, N=5 1110: DIV=32, N=6 1111: DIV=32, N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, indicating that a jump is generated by every N events.
31:8	Reserved		

13.6.9 Channel 2 capture/compare mode register (TMR2_CH2CCM)

Offset address: 0x20

Reset value: 0x0000 0000

Please refer to above CH1CCM register description.

Output compare mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel2 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI2

Field	Name	R/W	Description
			10: CC2 channel is input, and IC2 is mapped on TI1 11: Reserved Note: This bit can be written only when the channel is closed (TMR2_CHCTRL1 register CH2CCEN=0).
2	Reserved		
3	OCBEN	R/W	Output Compare Channel2 Preload Enable Please refer to CH1CCM_OCBEN.
6:4	OCMS	R/W	Output Compare Channel2 Mode Select Please refer to CH1CCM_OCMS.
31:7	Reserved		

Input capture mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel2 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI2 10: CC2 channel is input, and IC2 is mapped on TI1 11: Reserved Note: This bit can be written only when the channel is closed (TMR2_CHCTRL1 register CH2CCEN=0).
3:2	IC2PSC	R/W	Input Capture Channel2 Perscaler Configure Please refer to CH1CCM_IC1PSC.
7:4	ICFC	R/W	Input Capture Channel2 Filter Configure Please refer to CH1CCM_ICFC.
31:8	Reserved		

13.6.10 Channel 3 capture/compare mode register (TMR2_CH3CCM)

Offset address: 0x24

Reset value: 0x0000 0000

Please refer to above CH1CCM register description.

Output compare mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel3 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC3 channel is output 01: CC3 channel is input, and IC3 is mapped on TI3 10: Reserved 11: Reserved Note: This bit can be written only when the channel is closed (TMR2_CHCTRL1 register CH3CCEN=0).
2	Reserved		
3	OCBEN	R/W	Output Compare Channel3 Preload Enable Please refer to CH1CCM_OCBEN.

Field	Name	R/W	Description
6:4	OCMS	R/W	Output Compare Channel3 Mode Select Please refer to CH1CCM_OCMS.
31:7	Reserved		

Input capture mode:

Field	Name	R/W	Description
1:0	MODESEL	R/W	Capture/Compare Channel3 Mode Select This bit defines the input/output direction and selects the input pin. 00: CC3 channel is output 01: CC3 channel is input, and IC3 is mapped on TI3 10: Reserved 11: Reserved Note: This bit can be written only when the channel is closed (TMR2_CHCTRL1 register CH3CCEN=0).
3:2	IC2PSC	R/W	Input Capture Channel3 Perscaler Configure Please refer to CH1CCM_IC1PSC.
7:4	ICFC	R/W	Input Capture Channel3 Filter Configure Please refer to CH1CCM_ICFC.
31:8	Reserved		

13.6.11 Channel control register 1 (TMR2_CHCTRL1)

Offset address: 0x28

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CH1CCEN	R/W	Capture/Compare Channel1 Output Enable When CC1 is configured as output: 0: Disable output 1: Enable output When CC1 is configured as input: This bit determines whether the value CNT of the counter can capture and enter TMR2_CH1CC register 0: Disable capture 1: Enable capture
1	CH1CCP	R/W	Capture/Compare Channel1 Output Polarity Configure When CC1 channel is configured as output: 0: OC1 high level is valid 1: OC1 low level is valid When CC1 channel is configured as input: 0: Capture on the high level or rising edge of TI1FP1 1: Capture on the low level or falling edge of TI1FP1 When CC1 channel is configured as trigger: 0: Trigger on the high level or rising edge of TI1FP1 and TI2FP1 1: Trigger on the low level or falling edge of TI1FP1 and TI2FP1
3:2	Reserved		
4	CH2CCEN	R/W	Capture/Compare Channel2 Output Enable

Field	Name	R/W	Description
			Please refer to CHCTRL1_CH1CCEN
5	CH2CCP	R/W	Capture/Compare Channel2 Output Polarity Configure Please refer to CHCTRL1_CH1CCP
31:6	Reserved		

13.6.12 Channel control register 2 (TMR2_CHCTRL2)

Offset address: 0x2C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CH3CCEN	R/W	Capture/Compare Channel3 Output Enable Please refer to CHCTRL1_CH1CCEN
1	CH3CCP	R/W	Capture/Compare Channel3 Output Polarity Configure Please refer to CHCTRL1_CH1CCP
31:2	Reserved		

13.6.13 Counter register 1 (TMR2_CNT1)

Offset address: 0x30

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CNT[15:8]	R/W	Counter Value High
31:8	Reserved		

13.6.14 Counter register 0 (TMR2_CNT0)

Offset address: 0x34

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CNT[7:0]	R/W	Counter Value Low
31:8	Reserved		

13.6.15 Prescaler register (TMR2_PSC)

Offset address: 0x38

Reset value: 0x0000

Field	Name	R/W	Description
3:0	PSC	R/W	Prescaler Value Clock frequency of counter (CK_CNT)=$f_{CK\_PSC}/2^{PSC}$
31:4	Reserved		

13.6.16 Auto reload register 1 (TMR2_AUTORLD1)

Offset address: 0x3C

Reset value: 0x0000 00FF

Field	Name	R/W	Description
7:0	AUTORLD[15:8]	R/W	Auto Reload Value High When the value of auto reload is empty, the counter will not count.
31:8	Reserved		

13.6.17 Auto reload register 0 (TMR2_AUTORLD0)

Offset address: 0x40

Reset value: 0x0000 00FF

Field	Name	R/W	Description
7:0	AUTORLD[7:0]	R/W	Auto Reload Value Low When the value of auto reload is empty, the counter will not count.
31:8	Reserved		

13.6.18 Channel 1 capture/compare register 1 (TMR2_CH1CC1)

Offset address: 0x44

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[15:8]	R/W	Capture/Compare Channel1 Value High When the capture/compare channel 1 is configured as input mode: CC contains the counter value transmitted by the last input capture channel 1 event. When the capture/compare channel 1 is configured as output mode: CC1 contains the current load capture/compare register value Compare the value CC1 of the capture and compare channel 1 with the value CNT of the counter to generate the output signal on OC1.
31:8	Reserved		

13.6.19 Channel 1 capture/compare register 0 (TMR2_CH1CC0)

Offset address: 0x48

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[7:0]	R/W	Capture/Compare Channel1 Value Low Refer to TMR2_CH1CC1
31:8	Reserved		

13.6.20 Channel 2 capture/compare register 1 (TMR2_CH2CC1)

Offset address: 0x4C

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[15:8]	R/W	Capture/Compare Channel2 Value High Refer to TMR2_CH1CC1
31:8	Reserved		

13.6.21 Channel 2 capture/compare register 0 (TMR2_CH2CC0)

Offset address: 0x50

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[7:0]	R/W	Capture/Compare Channel2 Value Low Refer to TMR2_CH1CC1
31:8	Reserved		

13.6.22 Channel 3 capture/compare register 1 (TMR2_CH3CC1)

Offset address: 0x54

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[15:8]	R/W	Capture/Compare Channel3 Value High Refer to TMR2_CH1CC1
31:8	Reserved		

13.6.23 Channel 3 capture/compare register 0 (TMR2_CH3CC0)

Offset address: 0x58

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CC[7:0]	R/W	Capture/Compare Channel3 Value Low Refer to TMR2_CH1CC1
31:8	Reserved		

14 Basic Timer (TMR4)

14.1 Introduction

The basic timer TMR4 has an 8-bit counter, auto reload register, prescaler and trigger controller.

14.2 Main characteristics

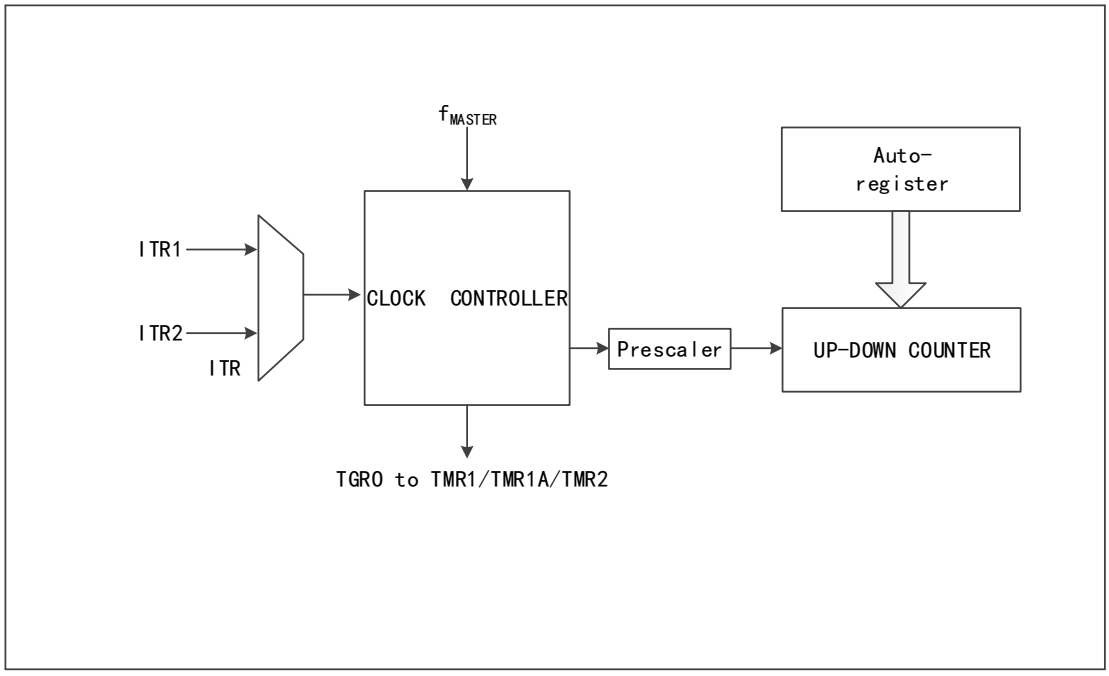
(1) Counter: 8-bit counter, which can only count up

(2) Prescaler: 3-bit programmable prescaler

(3) Clock source
- Internal clock
- External input

14.3 Structure block diagram

Figure 40 Basic Timer Structure Block Diagram



14.4 Functional Description

14.4.1 Clock source selection

Configure the CNTEN bit of TMR4_CTRL1 register to enable the counter; when CNTEN bit is set, the internal clock CK_INT can generate CK_INT to drive the counter through the controller and prescaler.

Internal clock

It is TMR2_CLK from RCM, namely the driving clock of the timer; when the slave mode controller is disabled, the clock source CK_PSC of the prescaler is driven by the internal clock CK_INT.

External clock mode 1

The trigger signal generated from the input channel of the timer after polarity selection and filtering is connected to the slave mode controller to control the work of the counter.

14.4.2 Time base unit

The time base unit in the basic timer contains three registers:

- 8-bit counter register (CNT)
- 8-bit auto reload register (AUTORLD)
- 3-bit prescaler register (PSC)

Counter CNT

The basic timer only has one count mode: count-up

Count-up mode

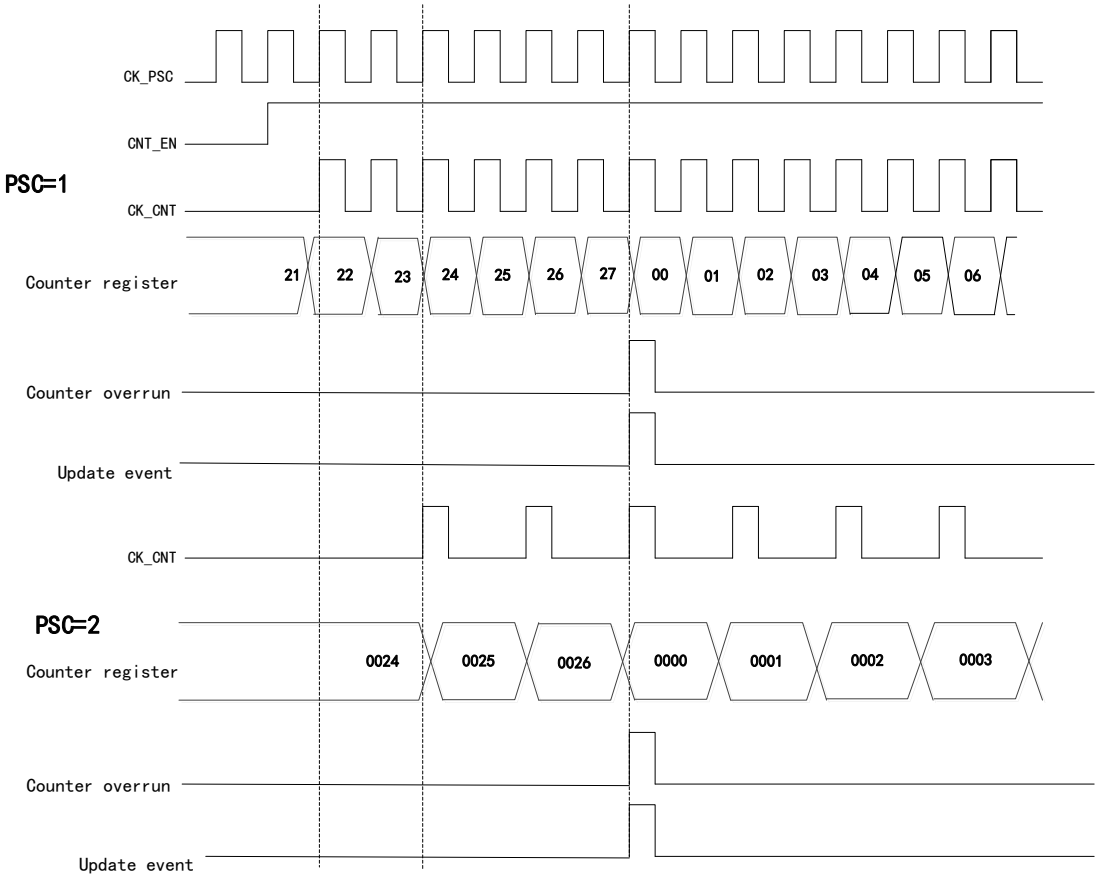
The counter counts up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMR4_CNT) is equal to the value of the auto reload (TMR4_AUTORLD), the counter will start to count from 0 again, a counter count-up overrun event will be generated, and the value of the auto reload (TMR4_AUTORLD) is written in advance.

Disable the update event and set NGUE bit of TMR4_CTRL1 register to 1.

Generate the update interrupt request and set UES bit in TMR4_CTRL1 register.

When an update event occurs, both the auto reload register and the prescaler register will be updated.

Figure 41 Timer Timing Diagram with Internal Clock Division Factor of 1 or 2



Prescaler PSC

The prescaler is programmable, and it can divide the clock frequency of the counter to any power of 2 between 1 and 128 (controlled by TMR4_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

14.5 Register address mapping

In the following table, all registers of TMR4 are mapped to a 16-bit addressable (address) space.

Table 31 Register Address Mapping

Register name	Description	Offset address
TMR4_CTRL1	Control register 1	0x00
TMR4_CTRL2	Control register 2	0x04
TMR4_SMC	Slave mode control register	0x08
TMR4_INTCTRL	Interrupt control register	0x0C
TMR4_STS	State register	0x10

Register name	Description	Offset address
TMR4_SCEG	Software control event generation register	0x14
TMR4_CNT	Counter register	0x18
TMR4_PSC	Prescaler register	0x1C
TMR4_AUTORLD	Auto reload register	0x20

14.6 Register functional description

14.6.1 Control register 1 (TMR4_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CNTEN	R/W	Counter Enable 0: Disable 1: Enable
1	NGUE	R/W	Update Disable Update event can cause AUTORLD and PSC to generate the value of update setting. 0: Enable update event (UEV) An update event can occur in any of the following situations: The counter overruns/underruns; Set UEG bit. 1: Disable update event
2	UES	R/W	Update Request Source Select If the interrupt is enabled, the update event can generate update interrupt request. Different update request sources can be selected through this bit. 0: The counter overruns 1: The counter overruns or underruns
3	SPMEN	R/W	Single Pulse Mode Enable When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the subsequent output level of the channel will not be changed. 0: Disable 1: Enable
6:4	Reserved		
7	ARBEN	R/W	Auto-reload Preload Enable 0: Disable 1: Enable
31:8	Reserved		

14.6.2 Control register 2 (TMR4_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	Reserved		
6:4	MMFC	R/W	Master Mode Signal Select The signals of timers working in master mode can be used for TRGO, which affects the work of timers in slave mode and cascaded with the master timer, and the specific impact is related to the configuration of slave mode timer. 000: Reset; the reset signal of master mode timer is used for TRGO 001: Enable; the counter enable signal of master mode timer is used for TRGO 010: Update; the update event of master mode timer is used for TRGO Others: Reserved
31:7	Reserved		

14.6.3 Slave mode control register (TMR4_SMC)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	SMFC	R/W	Slave Mode Function Select 000: Disable the slave mode, the timer can be used as master mode timer to affect the work of slave mode timer; if CTRL1_CNTEN=1, the prescaler is directly driven by the internal clock. 001~011: Reserved 100: Reset mode; the slave mode timer resets the counter after receiving the rising edge signal of TRGI and generates the signal to update the register. 101: Double-control mode 110: Single-control mode 111: External clock mode 1; select the rising edge signal of TRGI as the clock source to drive the counter to work.
3	Reserved		
6:4	ITC	R/W	Trigger Input Signal Select In order to avoid false edge detection when changing the value of this bit, it must be changed when SMFC=0. 000: Reserved 001: Internal trigger ITR1 connects to TMR1 TRGO 010: Internal trigger ITR0 connects to TMR1A TRGO 011: Internal trigger ITR3 connects to TMR2 TRGO 100~111: Reserved
7	MSMEN	R/W	Master/slave Mode Enable 0: Disable 1: Enable the master/slave mode
31:8	Reserved		

14.6.4 Interrupt control register (TMR4_INTCTRL)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	UDIE	R/W	Update interrupt Enable 0: Disable 1: Enable
5:1	Reserved		
6	TRGIE	R/W	Trigger Interrupt Enable 0: Disable 1: Enable
31:7	Reserved		

14.6.5 State register (TMR4_STS)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	UDIF	R/W	Update Event Interrupt Generate Flag 0: Update event interrupt does not occur 1: Update event interrupt occurs When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared to 0 by software.
5:1	Reserved		
6	TRGIF	R/W	Trigger Event Interrupt Generate Flag 0: Trigger event interrupt does not occur 1: Trigger event interrupt occurs When a trigger event is generated, this bit is set to 1 by hardware and cleared to 0 by software.
31:7	Reserved		

14.6.6 Software control event generation register (TMR4_SCEG)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	UEG	W	Update Event Generate 0: Invalid 1: Initialize the counter and generate the update event This bit is set to 1 by software, and cleared to 0 by hardware.
5:1	Reserved		
6	TEG	W	Trigger Event Generate 0: Invalid 1: Trigger event is generated This bit is set to 1 by software and cleared to 0 automatically by hardware.
31:7	Reserved		

14.6.7 Counter register (TMR4_CNT)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CNT	R/W	Counter Value
31:8	Reserved		

14.6.8 Prescaler register (TMR4_PSC)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	PSC	R/W	Prescaler Value Clock frequency of counter (CK_CNT)=$f_{CK\_PSC}/2^{PSC}$
31:3	Reserved		

14.6.9 Auto reload register (TMR4_AUTORLD)

Offset address: 0x20

Reset value: 0x0000 00FF

Field	Name	R/W	Description
7:0	AUTORLD	R/W	Auto Reload Value When the value of auto reload is empty, the counter will not count.
31:8	Reserved		

15 Watchdog Timer (WDT)

15.1 Introduction

The watchdog is used to monitor system failures caused by software errors. There are two watchdog devices on the chip: independent watchdog and window watchdog, which improve the security, and make the time more accurate and the application more flexible.

The independent watchdog will reset when the counter decreases to 0, and when the value on the counter is outside the window value, it will be reset if it is reloaded.

The window watchdog will reset when the counter decreases to 0x3F. When the count value of the counter is before the window value of the configuration register, the refresh counter will also be reset.

15.2 Independent watchdog

15.2.1 Introduction

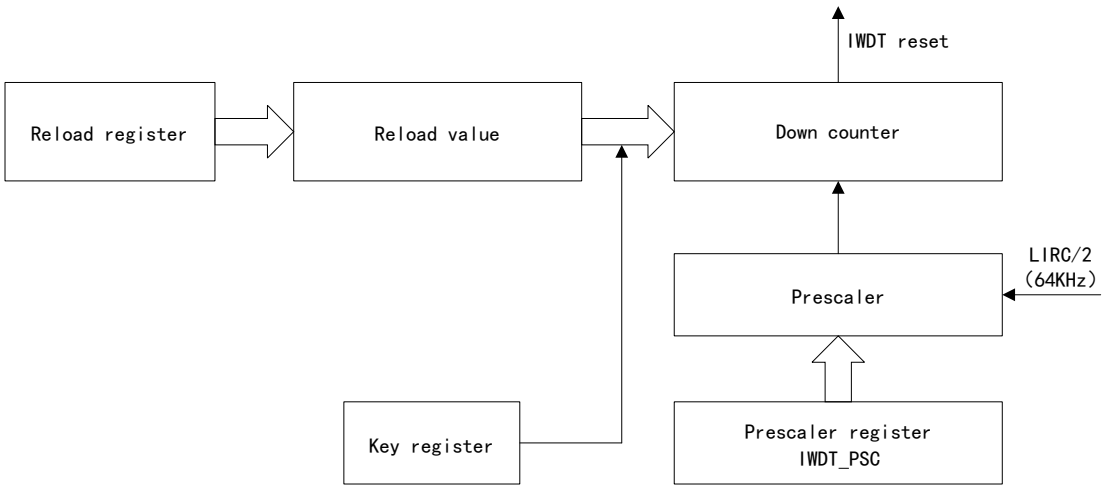
The independent watchdog consists of an 8-bit prescaler IWDT_PSC, 8-bit count-down counter, 8-bit reload register IWDT_CNTRLD, and keyword register IWDT_KEYWORD.

The independent watchdog has an independent clock source, and even if the master clock fails, it is still valid.

The independent watchdog is applicable to the situations where an independent environment is required but the accuracy requirement is not high.

15.2.2 Functional block diagram

Figure 42 Independent Watchdog Block Diagram



Note: The watchdog function is in the V_{DD} power supply area and can work normally in the stop or standby mode.

15.2.3 Functional Description

15.2.3.1 Key register

Write 0xAA in the key register to enable the independent watchdog, then the counter starts to count down from the reset value 0xFF and when the counter counts to 0x00, a reset will be generated.

Whenever the value of KEY_REFRESH (0xAA) is written to the IWDT_KEYWORD register, independent watchdog will use the value of IWDT_CNTRLD to refresh the contents of the counter, thus avoiding the reset of the watchdog.

IWDT_PSC and IWDT_CNTRLD registers have written protection function. Before modifying them, it is required to first write the KEY_ACCESS code value (0x55) in the IWDT_KEYWORD register; writing 0xAA in IWDT_KEYWORD will restore the write protection state.

15.2.3.2 Timeout period

The timeout period is configured by IWDT_PSC and IWDT_CNTRLD registers. It is determined by the following formula:

$$T=2*T_{LIRC}*P*R$$

Wherein: T = timeout period; T_{LIRC} = 1/f_{LIRC};

P = 2 ^(PSC [2:0] + 2) ； R = CNTRLD [7:0]+1

The IWDT counter must refresh the validity period by the software during the timeout period. Otherwise, the IWDT reset will be generated after the following delay time after the last refresh operation: D = t + 6 x T_{LIRC}

Wherein, D=delay between last refresh operation and IWDT reset.

Table 32 Watchdog Timeout Period (LIRC=128KHz)

PSC	Minimum timeout value (CNTRLD [7:0]=0x00)	Maximum timeout value (CNTRLD [7:0]=0xFF)
0	62.5 μs	15.90 ms
1	125 μs	31.90 ms
2	250 μs	63.70 ms
3	500 μs	127 ms
4	1.00 ms	255 ms
5	2.00 ms	510 ms
6	4.00 ms	1.02 s

15.2.3.3 Hardware watchdog

If the function of the hardware watchdog is enabled in the option byte, the function of the watchdog will be automatically turned on when the chip is powered on. If the software cannot operate IWDT_KEYWORD in time, a reset will be generated when the counter reaches 0x00.

15.3 Window watchdog

15.3.1 Introduction

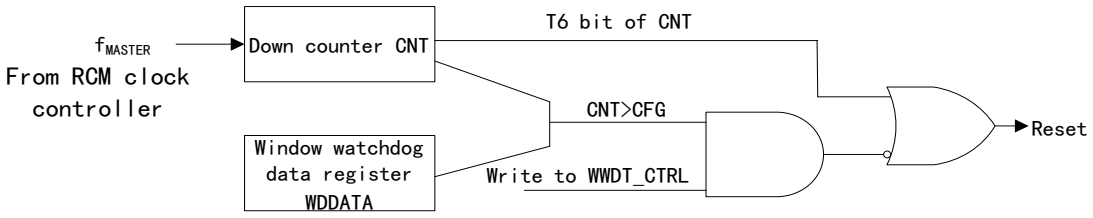
The window watchdog contains a 7-bit free-running down counter, control register WWDT_CTRL, and data register WWDT_WDDATA.

The window watchdog clock is from f_{MASTER}.

The window watchdog is applicable when precise timing is needed.

15.3.2 Functional block diagram

Figure 43 Window Watchdog Function Block Diagram



15.3.3 Functional Description

15.3.3.1 Reset

Enable window watchdog timer; the reset conditions are:

- When the counter count is less than 0x40, a reset will be generated.
- The reload counter will be reset before the counter counts to the value of the window register.

After reset, the watchdog is always closed and the watchdog can be turned on only by setting the WWDTEN bit of WWDT_CTRL register.

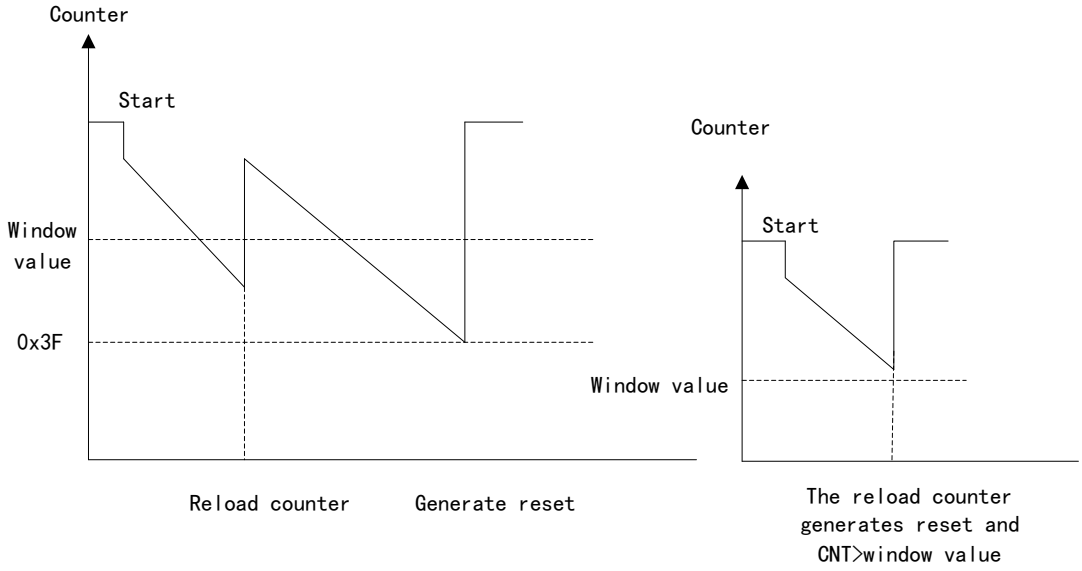
In order to avoid reset, the application program needs to periodically reassign values for WWDT_CTRL, under the condition that the value of the counter is less than the value of the window register. The assigned value is between 0xFF and 0xC0.

15.3.3.2 Timeout

The unique window of the window watchdog timer can effectively monitor whether the program is faulty. For example, assuming that the running time of a program segment is T, and the value of the window register is slightly less than

(TR-T), if there is no reload register in the window, it means that the program is faulty, and when the counter counts to 0x3F, it will generate reset.

Figure 44 Window Watchdog Timing Diagram



The calculation formula of window watchdog timer timeout is as follows:

$$T_{WWDT}=T_{MASTER}\times 12288\times（T[5:0]+1）$$

Wherein:

- T_{WWDT}: WWDT timeout period
- T_{PCLK1}: Peripheral clock cycle in ms

Note: To avoid generating reset immediately, it is required to always set CNT6 bit to 1 and then the WWDT_CTRL register can be operated.

15.3.3.3 Low-power mode

Table 33 Low-power Mode of Window Watchdog

Mode	WWDTRST in option byte	Description
Wait	-	Affected, the down counter works normally
Halt	0	No reset is generated, and MCU enters the stop mode. The counter stops counting after decreasing once until an interrupt is received. After a stable delay, the watchdog will resume counting. After the system is reset, the watchdog can be enabled only when the hardware watchdog is selected in the option byte.
	1	A reset is generated, and MCU does not enter the stop mode.

Mode	WWDTRST in option byte	Description
Active Halt	X	No reset is generated, and MCU enters the Active Halt mode. Stop counting until the oscillator interrupt or external interrupt is received, and then resume counting. After the CPU is reset, the watchdog needs to wait, and it will start to count when the oscillator is stable.

15.4 IWDT register address mapping

Table 34 Register Address Mapping of IWDT

Register name	Description	Offset address
IWDT_KEYWORD	Key register	0x00
IWDT_PSC	Prescaler register	0x04
IWDT_CNTRLD	Counter reload register	0x08

15.5 IWDT register functional description

These peripheral registers can be operated by half word (16 bits) or word (32 bits).

15.5.1 Key register (IWDT_KEYWORD)

Offset address: 0x00

Reset value: 0x0000 0000 (reset in standby mode)

Field	Name	R/W	Description
7:0	KEYWORD	W	Allow Access IWDT Register Key Value Writing 0x5555 means enabled access to IWDT_PSC, IWDT_CNTRLD and IWDT_WIN registers When the software writes 0xAAAA, it means to execute the reload counter, and a certain interval is required to prevent the watchdog from resetting. Write 0xCCCC and the watchdog will be enabled (the hardware watchdog is unrestricted by this command word). The read-out value is 0x0000.
31:8	Reserved		

15.5.2 Prescaler register (IWDT_PSC)

Offset address: 0x04

Reset value: 0x0000 0006

Field	Name	R/W	Description
2:0	PSC	R/W	Counter Clock Prescaler Factor 000: Four-divided frequency 001: 8 divided frequency 010: 16 divided frequency 011: 32 divided frequency 100: 64 divided frequency 101: 128 divided frequency 110: 256 divided frequency 111: Reserved
31:3	Reserved		

15.5.3 Counter reload register (IWDT_CNTRLD)

Offset address: 0x08

Reset value: 0x0000 00FF(reset in standby mode)

Field	Name	R/W	Description
7:0	CNTRLD	R/W	Watchdog Counter Reload Value Setup It has write-protection function and defines the value loaded to the watchdog timer when 0xAA is written to the IWDT_KEYWORD register. The watchdog timeout cycle can be calculated by the reload value and clock prescaler value.
31:8	Reserved		

15.6 WWDT register address mapping

Table 35 WWDT Register Address Mapping

Register name	Description	Offset address
WWDT_CTRL	Control register	0x00
WWDT_WDDATA	Window watchdog data register	0x04

15.7 WWDT register functional description

These peripheral registers can be operated by half word (16 bits) or word (32 bits).

15.7.1 Control register (WWDT_CTRL)

Offset address: 0x00

Reset value: 0x0000 007F

Field	Name	R/W	Description
6:0	CNT	R/W	Counter Value Setup This counter is 7 bits, and CNT6 is the most significant bit These bits are used to store the counter value of the watchdog. When the value decreases from 0x40 to 0x3F, WWDT reset will be generated.

Field	Name	R/W	Description
7	WWDTEN	R/S	Window Watchdog Enable This bit is set to 1 by software and can be cleared by hardware only after reset. When WWDTEN=1, WWDT can generate a reset. 0: Disable 1: Enable
31:8	Reserved		

15.7.2 Window watchdog data register (WWDT_WDDATA)

Offset address: 0x04

Reset value: 0x0000 007F

Field	Name	R/W	Description
6:0	WINCNT	R/W	Window Value Setup This window value is 7 bits, which is used to compare with the down counter.
31:7	Reserved		

16 Serial Peripheral Interface (SPI)

16.1 Introduction

Serial peripheral interface (SPI) provides data transmitting and receiving functions based on SPI protocol, which allows chips to communicate with external devices in half duplex, full duplex, synchronous and serial modes, and can work in master or slave mode.

16.2 Main characteristics

(1) Master and slave operation with 4-wire full duplex synchronous transmission and receiving

(2) Simplex synchronous transmission can be realized by two wires (the third bidirectional data line can be included/not included)

(3) Select 8-bit transmission frame format

(4) Select master or slave mode

(5) Fast communication in master/slave mode, up to 8Mbit/s

(6) Clock polarity and phase are programmable

(7) Data sequence is programmable; select MSB or LSB first

(8) Support special transmission and receiving mark and can trigger interrupt

(9) Have SPI bus busy state flag

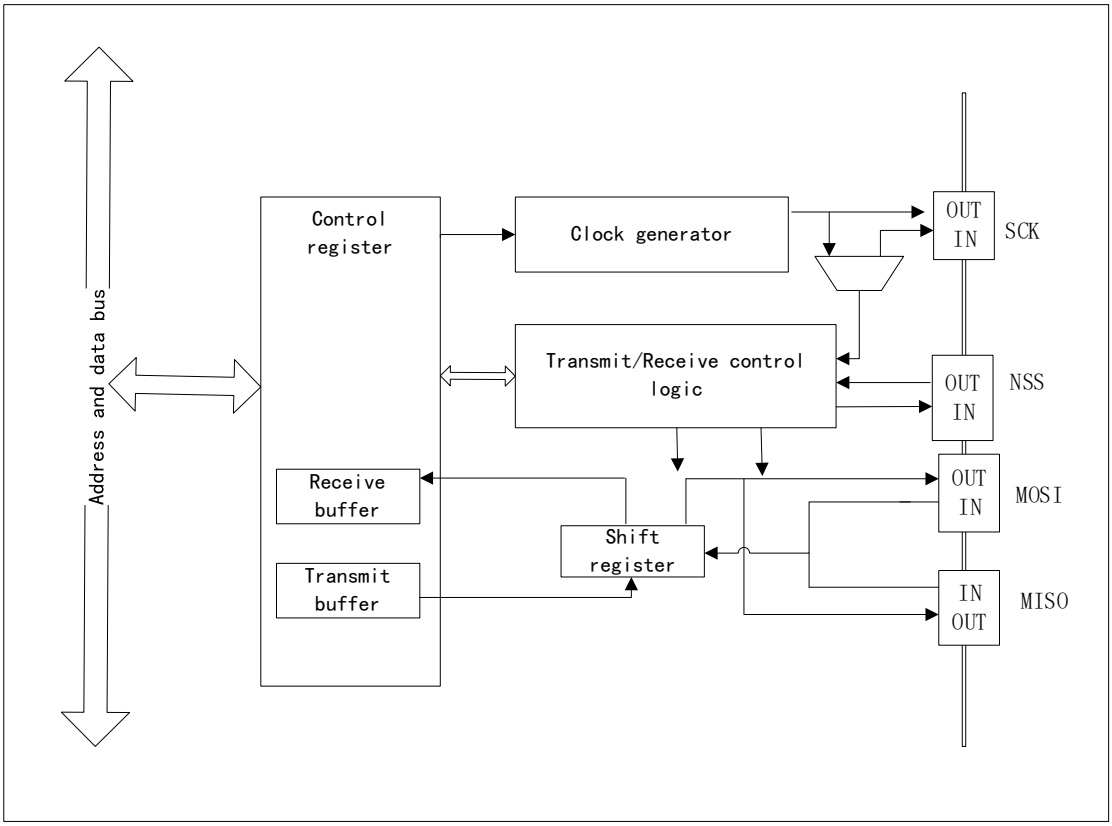
(10) Interrupt can be triggered by master mode fault and overrun flag

(11) Calculate, transmit and verify through hardware CRC

(12) Wakeup function; MCU can wake up from low-power mode in full or half duplex transmit-only mode

16.3 Structure block diagram

Figure 45 SPI Structure Block Diagram



16.4 SPI functional description

16.4.1 Description of SPI signal line

Table 36 SPI Signal Line Description

Pin name	Description
SCK	Master device: SPI clock outputs Slave device: SPI clock inputs
MISO	Master device: Input the pin and receive data Slave device: Output the pin and transmit data Data direction: From slave device to master device
MOSI	Master device: Output the pin and transmit data Slave device: Input the pin and receive data Data direction: From master device to slave device
NSS	Function-programmable pin. Its function is used as a "chip selection pin", so that the master device can communicate with the specific slave device separately to avoid conflicts on the data line. The NSS pin of the slave device can be driven by the standard IO of the master device.

16.4.2 Phase and polarity of clock signal

The clock polarity and clock phase are CPOL and CPHA bits of SPI_CTRL1

register.

Clock polarity CPOL means the level signal of SCK signal line when SPI is in idle state.

- When CPOL=0, SCK signal line is at low level in idle state
- When CPOL=1, SCK signal line is at high level in idle state

Clock phase CPHA means the sampling moment of data

- When CPHA=0, the signal on MOSI or MISO data line will be sampled by the "odd edge" on SCK clock line.
- When CPHA=1, the signal on MOSI or MISO data line will be sampled by the "even edge" on SCK clock line.

SPI can be divided into four modes according to the states of clock phase CPHA and clock polarity CPOL.

Table 37 Four Modes of SPI

SPI mode	CPHA	CPOL	Sampling moment	Idle SCK clock
0	0	0	Odd edge	Low level
1	0	1	Odd edge	High level
2	1	0	Even edge	Low level
3	1	1	Even edge	High level

16.4.3 Data frame format

Set MSB or LSB to be first by configuring LSBF bit in SPI_CTRL1 register.

16.4.4 NSS mode

The software NSS mode can be enabled by setting SSC bit of SPI_CTRL2 configuration register to 1, and the internal NSS signal level is set by the ISS bit of SPI_CTRL2 register.

16.4.5 SPI mode

16.4.5.1 SPI master mode

In master mode, generate serial clock on SCK pin.

Master mode configuration

- Configure MSTMODE=1 in SPI_CTRL1 register
- Set the clock baud rate by configuring BRC bit in SPI_CTRL1 register
- Select the polarity and phase by configuring CLKPOL and CLKPHA bits in SPI_CTRL1 register.
- Select LSB or MSB first by configuring LSBF in SPI_CTRL1 register
- NSS configuration:
  - In hardware mode, the NSS pin shall be connected at high level in the whole data frame transmission process

  - In software mode, the SSC bit and ISS bit in SPI_CTRL1 register shall be set
- Enable SPI by configuring SPIEN bit in SPI_CTRL1 register

In master mode: MOSI pin is data output, while MISO is data input.

16.4.5.2 SPI slave mode

In slave mode, SCK pin receives the serial clock transmitted from the master device.

Configuration of slave mode

- Configure MSTMODE=0 in SPI_CTRL1 register
- Select the polarity and phase by configuring CLKPOL and CLKPHA bits in SPI_CTRL1 register.
- Select LSB or MSB first by configuring LSBF in SPI_CTRL1 register
- NSS configuration:
  - In hardware mode: NSS pin must be at low level in the whole data frame transmission process
  - In software mode: Set SSC bit in SPI_CTRL1 register and clear ISS bit
- Enable SPI by configuring SPIEN bit in SPI_CTRL1 register

In slave mode: MOSI pin is data input, while MISO is data output.

16.4.5.3 Half-duplex communication of SPI

One clock line and one bidirectional data line

- Enable this mode by setting BMEN bit of SPI_CTRL1 register
- Control the data line to input or output by setting BMTX bit of SPI_CTRL1 register
- SCK pin is used as clock, MOSI pin is used in master device to transmit data, and MISO pin is used in slave device to transmit data

16.4.5.4 Simplex communication of SPI

One clock line and one unidirectional data line (duplex or receive-only)

Disable SPI output function by setting the UMRXO bit of SPI_CTRL2 register, and SPI will run in receive-only mode; then release the transmit pin (MOSI in master mode, and MISO in slave mode), and it can be used as other functions. When the UMRXO bit is cleared to 0, SPI will run in full-duplex mode.

Receive-only mode:

- In master mode, enable SPI to start communication, clear SPIEN pin of SPI_CTRL1 register, and it will stop receiving data immediately, not needing to read BUSYF flag (always 1 during communication).
- Slave mode: When NSS is pulled to low level, SPI will receive all the time as long as SCK has clock pulse.

16.4.6 Data transmission and receiving process in different SPI modes

Table 38 Run Mode of SPI

Mode	Configuration	Data pin
Full duplex mode of master device	BMEN=0, UMRXO=0	MOSI transmits; MISO receives
Unidirectional receiving mode of master device	BMEN=0, UMRXO=1	MOSI is not used; MISO receives
Bidirectional transmitting mode of master device	BMEN=1, BMTX=1	MOSI transmits; MISO is not used
Bidirectional receiving mode of master device	BMEN=1, BMTX=0	MOSI is not used; MISO receives
Full duplex mode of slave device	BMEN=0, UMRXO=0	MOSI receives, and MISO transmits
Unidirectional receiving mode of slave device	BMEN=0, UMRXO=1	MOSI receives, and MISO is not used
Bidirectional transmitting mode of slave device	BMEN=1, BMTX=1	MOSI is not used, and MISO transmits
Bidirectional receiving mode of slave device	BMEN=1, BMTX=0	MOSI receives, and MISO is not used

Figure 46 Connection in Full Duplex Mode

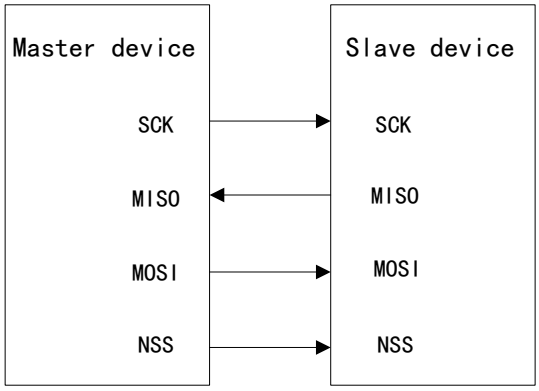


Figure 47 Connection in Simplex Mode (the master is used for receiving, while the slave is used for transmitting)

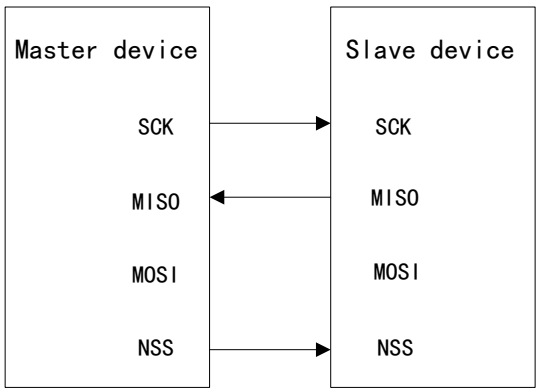


Figure 48 Connection in Simplex Mode (the master only transmits, while the slave receives)

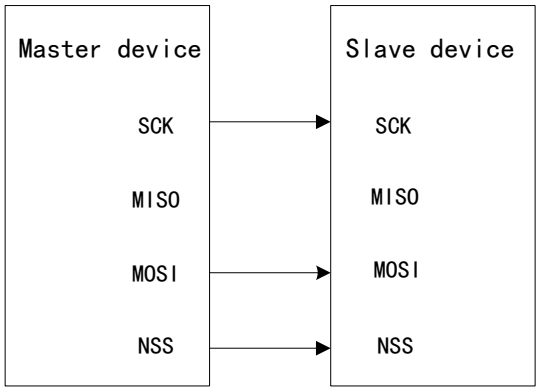
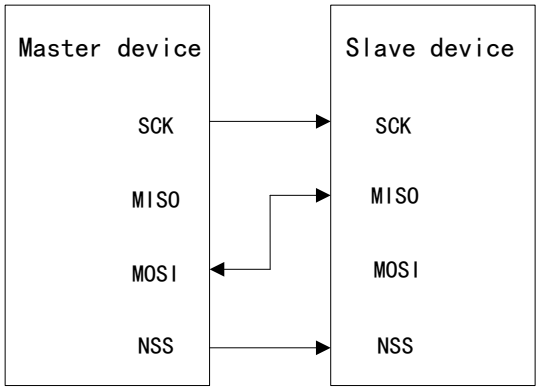


Figure 49 Bidirectional Line Connection



16.4.6.1 Transmitting and receiving of processed data

Data transmission

After the mode configuration is completed, the SPI module is enabled to remain idle.

Master mode: The software writes a data frame to the transmit buffer, and the transmission process starts

Slave mode: The SCK signal on the SCK pin starts to jump, while the NSS pin level is low, and the transmission process starts (before starting data transmission, make sure that the data has been written to the transmit buffer in advance).

When SPI is transmitting a data frame, it will load the data frame from the data buffer to the shift register, and then start to transmit data. After the data frame transmits one bit, TXBEF is set to 1; if TXBEIE bit of SPI_INTCTRL register is set, an interrupt will be generated.

Data receiving

BUSYF flag is always set to 1 in the data receiving process.

At the last edge of the sampling clock, the received data is transmitted from the shift register to the receive buffer; set the RXBNEF flag, and the software reads the data in data register (SPI_DATA) to obtain the content of the receive buffer; if RXBNEIE bit of SPI_INTCTRL register is set, an interrupt will be generated, and after data is read, the BUSYF flag will be automatically cleared.

16.4.7 CRC functions

SPI module contains two CRC computing units, which are used for data receiving and data transmission respectively.

CRC computing unit is used to define polynomials in SPI_CRCPOLY register.

Enable CRC computing by configuring CRCEN bit in SPI_CTRL2 register; at the same time, reset the CRC register (SPI_RXCRC and SPI_TXCRC).

To obtain the CRC value of transmission calculation, after the last data is written to the transmit buffer, it is required to set CRCNXT bit of SPI_CTRL2; indicate that the hardware transmits the CRC value after the last data is transmitted, and the CRCNXT bit will be cleared; at the same time, compare the values of CRC and SPI_RXCRC, and if they do not match, it is required to set CRCEF bit of SPI_STS register, and when ERRIE bit of SPI_INTCTRL register is set, an interrupt will occur.

Note: When the SPI clock frequency is too high, during the CRC transmission period, the CPU utilization frequency will be reduced, and the function call is disabled in the CRC transmission process to avoid errors when receiving the last data and CRC.

Sequence of clearing CRC values

(1) Disable SPI (SPIEN=0)

(2) Clear CRCEN bit to 0

(3) Set CRCEN bit to 1

(4) Enable SPI (SPIEN=1)

16.4.8 Disable SPI

After data transmission is over, end the communication by closing SPI module. In some configurations, if SPI is closed before data transmission is completed, data transmission error may be caused. Different methods are required in different operation modes to close SPI

Full duplex mode under master/slave device

(1) Wait until RXBNEF flag bit is set to 1, and receive the last data

(2) Wait until TXBEF flag bit is set to 1

(3) Wait until BUSYF flag bit is cleared to zero

(4) Close SPI (set SPIEN=0 of SPI_CTRL1 register)

Unidirectional/Bidirectional receive-only mode under master/slave device

(1) Wait until No. n-1 RXBNEF flag bit is set to 1

(2) Wait for one SPI clock cycle before SPI is closed (set SPIEN=0 of SPI_CTRL1 register)

(3) Before entering the stop mode, wait until the last RXBNEF flag bit is set to 1

Receive-only/Bidirectional receiving mode in slave mode

SPI can be closed at any time (set SPIEN=0 of SPI_CTRL1 register) and it will be closed when the transmission is over. If you want to enter the stop mode, wait until the BUSYF flag bit is cleared to zero.

16.4.9 Interrupt

16.4.9.1 State flag bit

There are three flag bits for fully monitoring the state of SPI bus.

Transmit buffer empty flag TXBEF

TXBEF=1 indicates that the transmit buffer bit is empty, and the next data to be transmitted can be written. When the data is written to SPI_DATA register, clear the TXBEF flag bit.

Receive buffer non-idle flag RXBNEF

RXBNEF=1 indicates that the receive buffer contains valid data and the data can be read through SPI_DATA register; and the RXBNEF flag can be cleared.

Busy flag BUSYF

BUSYF flag is set and cleared by hardware, which can indicate the state of SPI communication layer. When BUSYF=1, it indicates SPI is communicating.

BUSYF flag can be used to detect whether transmission is over to avoid damaging the last transmitted data.

BUSYF flag bit can be used to avoid conflict when writing data in multi-master mode.

BUSYF flag will be cleared to zero when the transmission ends (except for continuous communication in master mode), SPI is closed and the master mode fails.

16.4.9.2 Error flag bit

Master mode error MMEF

MMEF is an error flag bit. The master mode error occurs when: in hardware NSS mode, the NSS pin of the master device is pulled down; in software NSS mode, ISS bit is cleared to zero; MMEF bit is set automatically.

Effect of master mode failure: MMEF is set to 1, and if ERRIE is set, SPI interrupt will be generated; SPIEN is cleared to zero (output stops, SPI interface is closed); MSTMODE is cleared to zero and the device is forced to enter the slave mode.

Operation of clearing the MMEF flag bit: When MMEF flag bit is set to 1, it is required to read or write SPI_STS register, and then write to SPI_CTRL1 register.

When MMEF flag bit is 1, it is not allowed to set SPIEN and MSTMODE bits.

Overflow error RXOF

Overrun error: After the master device transmits the data, the RXBNEF flag bit is still 1, which indicates that the overrun error occurred. Then RXOF bit is set to 1, and if the ERRIE bit is also set, an interrupt will be generated.

After an overrun error occurs, the data in the receive buffer is not the data transmitted by the master device, and then the read data in SPI_DATA register is the data not read before, while the data transmitted later will not be read.

RXOF flag can be cleared by reading SPI_DATA register and SPI_STS register according to the sequence.

CRC error flag CRCEF

By setting CRCEN bit of SPI_CTRL2 register, start CRC computing, and CRC error flag can check whether the received data is valid.

When the value transmitted by SPI_TXCRC register does not match the value in SPI_RXCRC register, a CRC error will be generated, and CRCEF flag bit in SPI_STS register will be set to 1.

CRCEF can be cleared by writing 0 to CRCEF bit of SPI_STS register.

Table 39 SPI Interrupt Request

Interrupt flag	Interrupt event	Enable control bit	Whether to exit the wait mode	Whether to exit the stop mode
TXBEF	Transmit buffer empty	TXBEIE	Yes	No

Interrupt flag	Interrupt event	Enable control bit	Whether to exit the wait mode	Whether to exit the stop mode
RXBNEF	Receive buffer not empty	RXBNEIE	Yes	No
WUPF	Wakeup event	WUPIE	Yes	Yes
MMEF	Mode error event	ERRIE	Yes	No
RXOF	Overflow error		Yes	No
CRCEF	CRC error		Yes	No

16.4.10 Low power

SPI in low-power mode

Wait mode: It has no impact on SPI. SPI interrupt will wake up the device from wait mode.

Stop mode: SPI register is frozen; in stop mode, SPI is inactive. If SPI is in master mode, the "wakeup from stop mode" interrupt can wake up the device to continue the communication; if SPI is in slave mode, it will wake up from stop mode when the sampling edge of the first data is detected.

Wake up the device from stop mode using SPI

In full-duplex or transmit-only half-duplex mode, when the MCU is in stop mode, SPI is the slave device, and as long as the NSS pin is still connected to low level or ISS bit is still reset before entering the Halt mode, it can respond to the communication.

When the first sampling edge of data is detected (defined by CLKPHA bit)

- Set WUPF bit in SPI_STS register
- If WUPIE bit in SPI_INTCTRL register is set to 1, an interrupt will be generated
- This interrupt can wake up the device from wait mode
- Since it takes time to recover the system clock, SPI will transmit/receive some data before correct communication. Therefore, the following steps shall be followed:
  - First, write a special value into SPI_DATA before entering stop mode. This value tells the external master device that this SPI enters the stop mode.
  - Then the external master device continuously transmits this special value until it receives a new data value, indicating that the SPI slave device has been awakened and can communicate correctly.

In receive-only mode (BMEN=0 and UMRXO=1 or BMEN=1 and BMTX=0), since the time required to recover the system clock may be greater than the

data receiving time, the received data may be lost, and the slave device cannot indicate to the master device which data have been correctly received.

16.5 Register address mapping

Table 40 Register Address Mapping

Register name	Description	Offset address
SPI_CTRL1	SPI control register 1	0x00
SPI_CTRL2	SPI control register 2	0x04
SPI_INTCTRL	SPI interrupt control register	0x08
SPI_STS	SPI state register	0x0C
SPI_DATA	SPI data register	0x10
SPI_CRCPOLY	SPI CRC polynomial register	0x14
SPI_RXCRC	SPI receive CRC register	0x18
SPI_TXCRC	SPI transmit CRC register	0x1C

16.6 Register functional description

16.6.1 SPI control register 1 (SPI_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CLKPHA	R/W	Clock Phase Configure This bit indicates on the edge of which clock to start sampling 0: On the edge of No. 1 clock 1: On the edge of No. 2 clock Note: This bit cannot be modified during communication.
1	CLKPOL	R/W	Clock Polarity Configure Level state maintained by SCK when SPI is in idle state. 0: Low level 1: High level Note: This bit cannot be modified during communication
2	MSTMODE	R/W	Master/Salve Mode Configure 0: Configure as slave mode 1: Configure as master mode Note: This bit cannot be modified during communication
5:3	BRC	R/W	Baud Rate Divider Factor Select 000: DIV=2 001: DIV=4 010: DIV=8 011: DIV=16 100: DIV=32

Field	Name	R/W	Description
			101: DIV=64 110: DIV=128 111: DIV=256 Baud rate=F_{MASTER}/DIV Note: These bits cannot be modified during communication
6	SPIEN	R/W	SPI Device Enable 0: Disable 1: Enable Note: This bit cannot be modified during communication
7	LSBF	R/W	LSB First Transfer Select 0: First transmit the most significant bit (MSB) 1: First transmit the least significant bit (LSB) Note: This bit cannot be modified during communication
31:8	Reserved		

16.6.2 SPI control register 2 (SPI_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	ISS	R/W	Internal Slave Device Select When SSC=1 (software NSS mode), select internal NSS level by configuring the bit 0: Slave mode; internal NSS is low 1: Master mode; internal NSS is high
1	SSC	R/W	Software Slave Device Enable 0: Disable software NSS mode 1: Enable software NSS mode, and the value of ISS bit replaces the level value of internal NSS pin
2	UMRXO	R/W	Receive Only Mode Enable 0: Transmit and receive at the same time 1: Receive-only mode This bit and BMEN bit together determine the transmission direction in the two-line and two-way mode. In the configuration of multiple slave devices, in order to avoid data transmission collision, it is necessary to set this bit to 1 on the slave devices that are not accessed.
3	Reserved		
4	CRCNXT	R/W	CRC Transfer Next Enable 0: The next transmitted data is from transmit buffer 1: The next transmitted data is from CRC register
5	CRCEN	R/W	CRC Calculate Enable 0: Disable 1: Enable CRC check function only applies to full duplex mode; only when SPIEN=0, can this bit be changed.

Field	Name	R/W	Description
6	BMTX	R/W	Bidirectional Mode Output Enable 0: Disable, namely, receive-only mode 1: Enable, namely, transmit-only mode When BMEN=1, namely, in single-line/double-line mode, this bit decides the transmission direction of transmission line.
7	BMEN	R/W	Bidirectional Mode Enable 0: Double-line unidirectional mode 1: Single-line bidirectional mode Single-line bidirectional transmission means: transmission between MOSI pin of data master and MISO pin of slave.
31:8	Reserved		

16.6.3 SPI interrupt control register (SPI_INTCTRL)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	Reserved		
4	WUPIE	R/W	Wake up Interrupt Enable 0: Disable 1: Enable When WUPF flag bit is set to 1, an interrupt request will be generated
5	ERRIE	R/W	Error interrupt Enable 0: Disable 1: Enable When an error occurs, this bit controls whether to generate the interrupt.
6	RXBNEIE	R/W	Receive Buffer Not Empty Interrupt Enable 0: Disable 1: Enable When RXBNEF flag bit is set to 1, an interrupt request will be generated
7	TXBEIE	R/W	Transmit Buffer Empty Interrupt Enable 0: Disable 1: Enable When TXBEF flag bit is set to 1, an interrupt request will be generated
31:8	Reserved		

16.6.4 SPI state register (SPI_STS)

Offset address: 0x0C

Reset value: 0x22C

Field	Name	R/W	Description
0	RXBNEF	R	Receive Buffer Not Empty Flag 0: Empty 1: Not empty
1	TXBEF	R	Transmit Buffer Empty Flag 0: Not empty 1: Empty
2	Reserved		
3	WUPF	RC_W0	Wake up Event Occur Flag 0: Not occur 1: Occur
4	CRCEF	RC_W0	CRC Error Occur Flag This bit indicates whether the received CRC value matches the value of RXCRC register 0: Match 1: Not match This bit is set by hardware, and it can be cleared by writing 0 to this bit by software.
5	MMEF	RC_W0	Mode Error Occur Flag 0: Not occur 1: Occur This bit is set by hardware, and it can be cleared by writing 0 to this bit by software.
6	RXOF	RC_W0	Overrun Occur Flag 0: Not occur 1: Occur This bit is set by hardware, and it can be cleared by writing 0 to this bit by software.
7	BUSYF	R	SPI Busy Flag 0: SPI is idle 1: SPI is communicating It is set or cleared by hardware.
31:8	Reserved		

16.6.5 SPI data register (SPI_DATA)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DATA	R/W	Transmit Receive Data register When writing this register, the data will be written to the transmit buffer; when reading this register, the data in receive buffer will be read.
31:8	Reserved		

16.6.6 SPI CRC polynomial register (SPI_CRCPOLY)

Offset address: 0x14

Reset value: 0x0000 0007

Field	Name	R/W	Description
7:0	CRCPOLY	R/W	CRC Polynomial Value Setup This register contains CRC polynomial of CRC computing, which can be modified, and the reset value is 0x0007.
31:8	Reserved		

16.6.7 SPI receive CRC register (SPI_RXCRC)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	RXCRC	R	Receive Data CRC Value The CRC data of the received data calculated by the hardware is stored in this register. When the CRCEN is set, the hardware will clear this register. Note: When BUSYF bit is set to 1, the value of reading this register may be wrong.
31:8	Reserved		

16.6.8 SPI transmit CRC register (SPI_TXCRC)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	TXCRC	R	Transmit Data CRC Value The CRC data of the transmitted data calculated by the hardware is stored in this register. When the CRCEN is set, the hardware will clear this register. Note: When BUSYF bit is set to 1, the value of reading this register may be wrong.
31:8	Reserved		

17 Universal Synchronous/Asynchronous Transceiver (USART)

17.1 Full Name and Abbreviation Description of Terms

Table 41 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Most Significant Bit	MSB
Least Significant Bit	LSB

17.2 Introduction

USART (universal synchronous/asynchronous receiver transmitter) is a serial communication device that can flexibly exchange full-duplex and half-duplex data with external devices, and meets the requirements of external devices for industry standard NRZ asynchronous serial data format. USART also provides a wide range of baud rate for selection and supports multiprocessor communication.

USART not only supports standard asynchronous transceiver mode, but also supports some other serial data exchange modes, such as LIN protocol, smart card protocol and IrDA SIR ENDEC specification.

17.3 Main characteristics

(1) Full duplex asynchronous communication

(2) Single-line half-duplex communication

(3) NRZ standard format

(4) Characteristics of programmable serial port:
- Data bit: 8 or 9 bits
- Check bits: Even parity check, odd parity check, no check
- Support 1, 1.5 and 2 stop bits

(5) Check control
- Transmit the check bit
- Check the received data

(6) Independent transmitter and receiver enable bit

(7) Programmable baud rate generator, with baud rate of up to 2.5Mbits/s

(8) Multiprocessor communication:

- If the address does not match, it will enter the mute mode
- Wake up from mute mode through idle bus detection or address flag detection

(9) Synchronous transmission mode

(10) Generation and detection of LIN break frame

(11) Support the smart card interface of ISO7816-3 standard

(12) Support IrDA protocol

(13) State flag bit:
- Transmission detection flag: The transmit register is empty, the receive register is not empty, and transmission is completed
- Error detection flag: Overrun error, noise error, parity check error, frame error

(14) Multiple interrupt sources:
- The transmit register is empty
- Transmission is completed
- The receive register is not empty
- Overrun error
- Bus idle
- Parity check error
- LIN disconnection detection

17.4 Functional Description

Table 42 USAR Pin Description

Pin	Type	Description
USART_RX	Input	Data receiving
USART_TX	Output I/O (single-line half-duplex)	Data transmission In single-line half-duplex mode, bidirectional communication is supported
USART_CK	Output	Clock output

17.4.1 Single-line half-duplex communication

HDMEN bit of USART_CTRL5 register determines whether to enter the single-line half-duplex mode.

When USART enters single-line half-duplex mode:
- The CLKEN and LINEN bits of USART_CTRL3 register, and IRDAEN and SMEN bits of USART_CTRL5 register must be cleared to 0.
- RX pin is disabled.
- TX pin should be configured as open-drain output and connected with RX pin inside the chip.

- Transmitting data and receiving data cannot be carried out at the same time. The data cannot be received before they are transmitted. If needing to receive data, enabling receiving can be turned on only after TXCF bit of USART_STS register is set to 1.
- If there is data collision on the bus, software is required to manage the distributed communication process.

17.4.2 Frame format

The frame format of data frame is controlled by USART_CTRL1 register

- DBL bit controls the character length, which can be set to 8 or 9 bits.
- PEN bit controls to turn on the check bit or not.
- PSEL bit controls the check bit to be odd or even.

The stop bits can be configured by SBS bit of USART_CTRL3 register.

Table 43 Frame Format

DBL bit	PEN bit	USART data frame
0	0	Start bit+8-bit data+stop bit
0	1	Start bit+7-bit data+parity check bit+stop bit
1	0	Start bit+9-bit data+stop bit
1	1	Start bit+8-bit data+ parity check bit+stop bit

Check bit

PSEL bit of USART_CTRL1 determines the parity check bit; when PSEL=0, it is even parity check, on the contrary, it is odd parity check.

- Even parity check: When the number of frame data and check bit 1 is even, the even parity check bit is 0; otherwise it is 1.
- Odd parity check: When the number of frame data and check bit 1 is even, the odd parity check bit is 1; otherwise it is 0.

17.4.3 Transmitter

When TXEN bit of the register USART_CTRL2 is set, the transmit shift register will output data through TX pin and the corresponding clock pulses will be output through CK pin.

17.4.3.1 Character transmission

During transmission period of USART, the least significant bit of the data will be moved out by TX pin first. In this mode, USART_ DATA register has a buffer between the internal bus and the transmit shift register.

A data frame is composed of the start bit, character and stop bit, so there is a low-level start bit in front of each character; then there is a high-level stop bits the number of which is configurable.

Transmission configuration steps

- Clear USARTDIS bit of USART_CTRL1 register to enable USART.
- Decide the word length by setting DBL bit of USART_CTRL1 register.
- Decide the number of stop bits by setting SBS bit of USART_CTRL3 register.
- Set the baud rate of communication in USART_BR register.
- Enable TXEN bit of USART_CTRL2 register, and transmit an idle frame.
- Wait for TXBEF bit of USART_STS register to be set to 1.
- Write data to USART_DATA register
- Wait for TXCF bit of USART_STS register to be set to 1, indicating transmission completed.

Note: TXEN bit cannot be reset during data transmission; otherwise, the data on TX pin will be destroyed, which is because if the baud rate generator stops counting, the data being transmitted will be lost.

17.4.3.2 Single-byte communication

TXBEF bit can be cleared to 0 by writing USART_DATA register. When the TXBEF bit is set by hardware, the shift register will receive the data transmitted from the data transmit register, then the data will be transmitted, and the data transmit register will be cleared. The next data can be written in the data register without overwriting the previous data.

(1) If TXIE in USART_CTRL2 register is set to 1, an interrupt will be generated.

(2) If USART is in the state of transmitting data, write to the data register to save the data to the DATA register, and transfer the data to the shift register at the end of the current data transmission.

(3) If USART is in idle state, write to the data register, put the data into the shift register, start transmitting data, and set TXBEFLG bit to 1.

(4) When a data transmission is completed and TXBEF bit is set, TXCF bit will be set to 1; at this time if TXCIE bit in USART_CTRL2 register is set to 1, an interrupt will be generated.

(5) After the last data is written in the USART_DATA register, before entering the low-power mode or before closing the USART module, wait to set TXCF to 1.

17.4.3.3 Break frame

The break frames are considered to receive 0 in a frame period. Setting TXBRK bit of USART_CTRL2 register can transmit a break frame, and the length of the break frame is determined by DBL bit of USART_CTRL1 register. If the TXBRK bit is set, after completion of transmission of current data, the TX line will transmit a break frame, and after completion of transmission of break frame, the TXBRK bit will be reset. At the end of the break frame, the transmitter inserts one or two stop bits to respond to the start bit.

Note: If the TXBRK bit has been reset before transmission of the break frame starts, the break frame will not be transmitted. To transmit two consecutive break frames, the TXBRK bit shall be set after the stop bit of the previous disconnection symbol.

17.4.3.4 Idle frame

The idle frame is regarded as a complete data frame composed entirely of 1, followed by the start bit of the next frame containing the data. Set TXEN bit of USART_CTRL2 register to 1 and one idle frame can be transmitted before the first data frame.

17.4.4 Receiver

17.4.4.1 Character receiving

During receiving period of USART, RX pin will first introduce the least significant bit of the data. In this mode, USART_ DATA register has a buffer between the internal bus and the receive shift register. The data is transmitted to the buffer bit by bit. When fully receiving the data, the corresponding receive register is not empty, then the user can read USART_ DATA.

Receiving configuration steps

- Set USARTDIS bit of USART_CTRL1 register to enable USART.
- Decide the word length by setting DBL bit of USART_CTRL1 register.
- Decide the number of stop bits by setting SBS bit of USART_CTRL3 register.
- Set the baud rate of communication in USART_BR register.
- Set RXEN bit of USART_CTRL2 to enable receiving.

Note: RXEN bit cannot be reset during data receiving period; otherwise, the bytes being received will be lost.

17.4.4.2 Break frame

When the receiver receives a break frame, USART will handle it as receiving a frame error.

17.4.4.3 Idle frame

When the receiver receives an idle frame, USART will handle it as receiving an ordinary data frame; if IDLEIE bit of USART_CTRL2 is set, an interrupt will be generated.

17.4.4.4 Overrun error

When RXBNEF bit of USART_STS register is set to 1 and a new character is received at the same time, an overrun error will be caused. Only after RXEN is reset, can the data be transferred from the shift register to DATA register.

When an overrun error occurs

- OEF bit of USART_STS will be set to 1.

- The data in DATA register will not be lost.
- The data in the shift register received before will be overwritten, but the data received later will not be saved.
- If RXIE bit of USART_CTRL2 is set to 1, an interrupt will be generated.
- The OEF bit can be reset by reading USART_STS and USART_DATA registers.

17.4.4.5 Noise error

When noise is detected in receiving process of the receiver:

- Set NE flag on the rising edge of RXBNEF bit of USART_STS register.
- Invalid data is transmitted from the shift register to USART_DATA register.

17.4.4.6 Frame error

If the stop bit is not received and recognized at the expected receiving time due to excessive noise or lack of synchronization, a frame error will be detected.

When a frame error is detected in receiving process of the receiver:

(1) Set the FEF bit of USART_STS register.

(2) Invalid data is transmitted from the shift register to USART_DATA register.

(3) No interrupt will be generated during single-byte communication.

17.4.5 Baud rate generator

Relationship between baud rate and system clock:

$$\text{Baud rate}=f_{MASTER}/(\text{USART\_DIV})$$

USART_DIV is an unsigned integer, which is stored in the registers BR1 and BR0.

17.4.6 Multiprocessor communication

In multiprocessor communication, multiple USART are connected to form a network. In this network, two devices communicate with each other, and the mute mode can be enabled for other devices not participating in the communication to reduce the burden of USART. In mute mode, no receive state bit will be set and all receive interrupts are disabled.

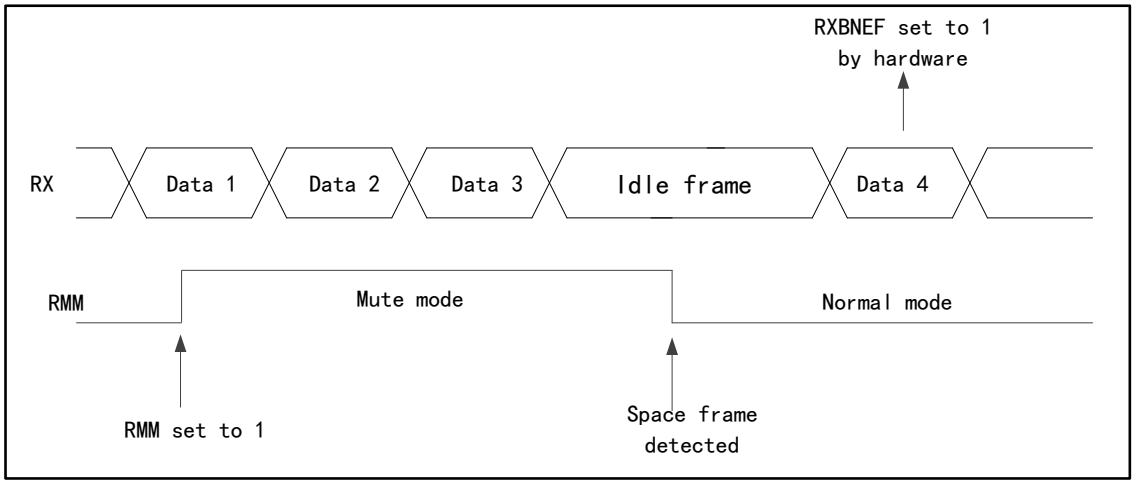
When mute mode is enabled, there are two ways to exit the mute mode:

- WMS bit is cleared and when the bus is idle, it can exit the mute mode.
- WMS bit is set and after receiving the address flag, it can exit the mute mode.

Idle bus detection (WMS=0)

When RMM is set to 1, USART enters the mute mode, and it can wake up from the mute mode when an idle frame is detected, meanwhile, the RMM bit will be cleared to 0 by hardware. RMM can also be cleared to 0 by software.

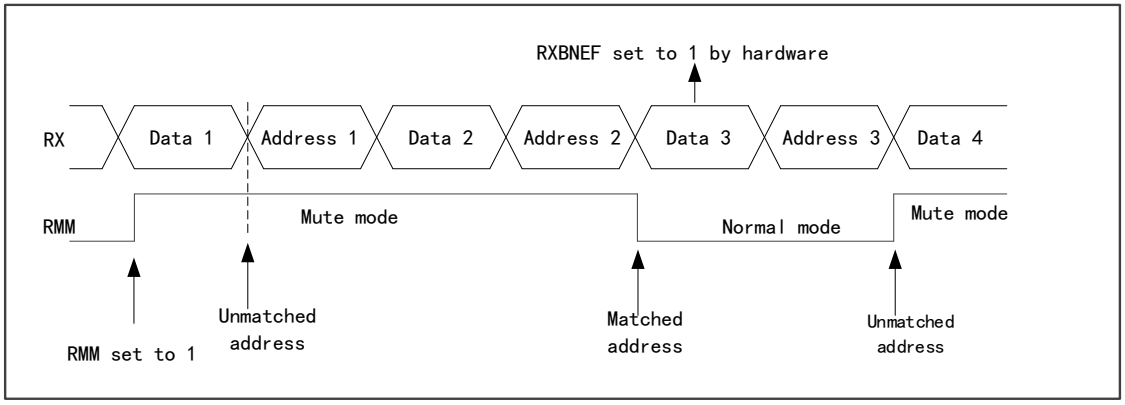
Figure 50 Idle Bus Exit Mute Mode



Address flag detection (WMS=1)

If the address flag bit is 1, this byte is regarded as the address. The storage address of lower four bits of the address bytes will first be compared with its own address when the receiver receives the address byte. If the addresses do not match, the receiver will enter the mute mode. If the addresses match, the receiver will wake up from the mute mode and be ready to receive the next byte. If the address byte is received again after exiting the mute mode, but the address does not match its own address, the receiver will enter the mute mode again.

Figure 51 Address Flag Exit Mute Mode



17.4.7 Synchronous mode

The synchronous mode supports full duplex synchronous serial communication in master mode, and has one more signal line USART_CK which can output

synchronous clock than the asynchronous mode.

CLKEN bit of USART_CTRL3 register decides whether to enter the synchronous mode.

When USART enters the synchronous mode:

- The LINEN bit of USART_CTRL3 register, and IRDAEN, HDMEN and SMEN bits of USART_CTRL5 register must be cleared to 0.
- The start bit and stop bit of data frame have no clock output.
- Whether the last data bit of data frame generates USART_CK clock is decided by the LBCP bit of USART_CTRL3 register.
- The clock polarity of USART_CK is decided by CLKPOL bit of USART_CTRL3 register.
- The phase of USART_CK is decided by the CLKPHA bit of USART_CTRL3 register.
- The external CK clock cannot be activated when the bus is idle or the frame is disconnected.

Figure 52 USART Synchronous Transmission Example

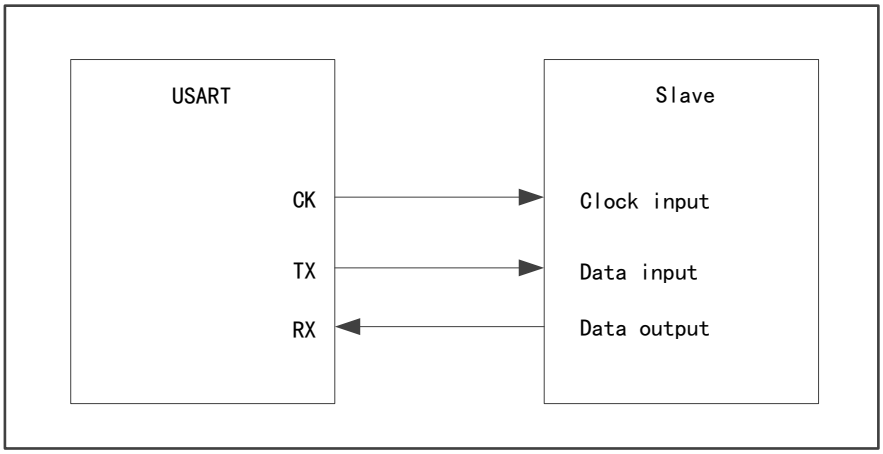


Figure 53 USART Synchronous Transmission Timing Diagram (DBL=0)

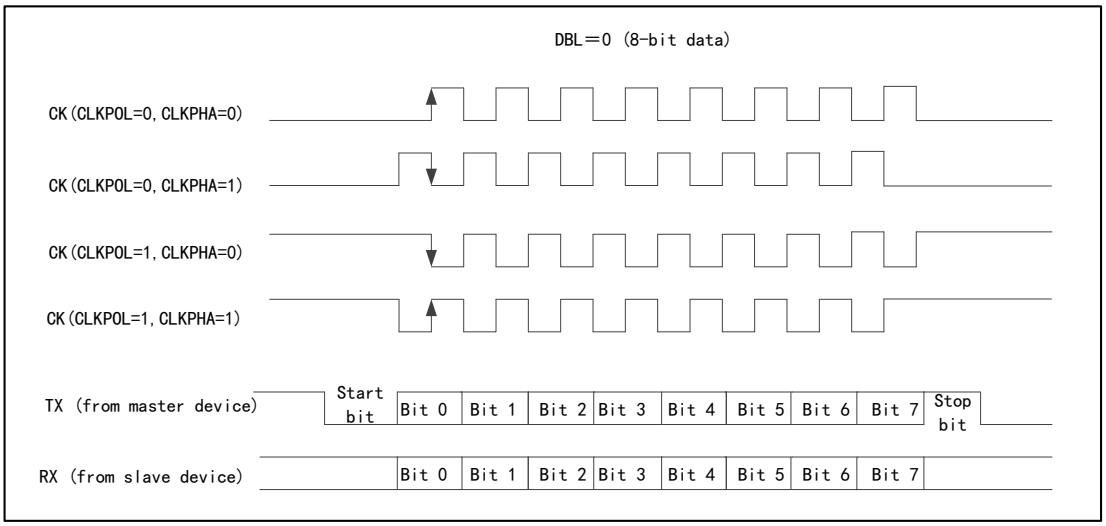
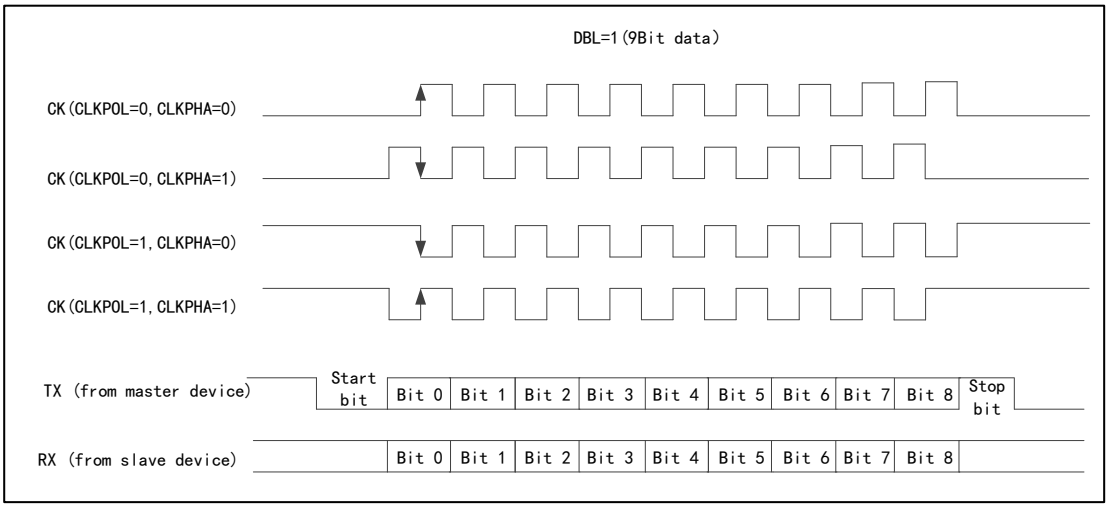


Figure 54 USART Synchronous Transmission Timing Diagram (DBL=1)



17.4.8 LIN mode

LINEN bit of USART_CTRL3 register decides whether to enter the LIN mode.

When entering LIN mode:

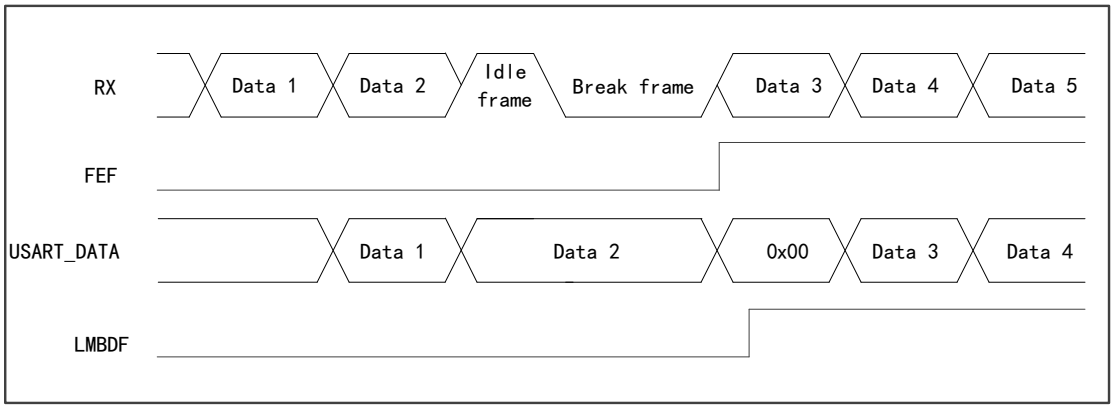
- All data frames are 8 data bits and 1 stop bit.
- The CLKEN and SBS bits of USART_CTRL3 register, and IRDAEN, HDMEN and SMEN bits of USART_CTRL5 register shall be cleared to 0.

In LIN master mode, USART can generate break frame, and the detection length of break frame can be set to 10 bits and 11 bits through LMBDL bit of USART_CTRL4. The break frame detection circuit is independent of USART receiver, and no matter in idle state or in data transmission state, RX pin can detect the break frame, and LMBDF bit of USART_CTRL4 register is set to 1; at this time, if LMBDIE bit of USART_CTRL4 is enabled, an interrupt will be generated.

Detection of break frame in idle state

In idle state, if a break frame is detected on RX pin, the receiver will receive a data frame of 0 and generate FEF.

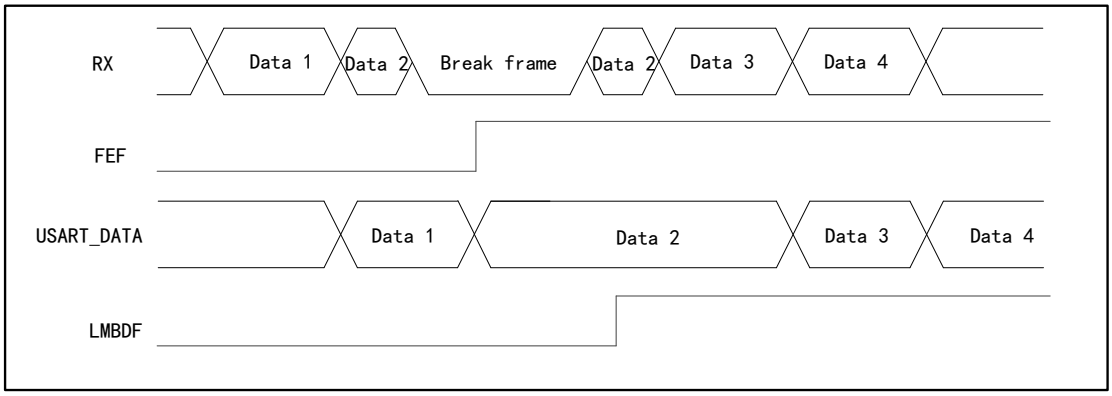
Figure 55 Break Frame Detection in Idle State



Detection of break frame in data transmission state

In the process of data transmission, if the RX pin detects the break frame, the currently transmitted data frame will generate FEF.

Figure 56 Break Frame Detection in Data Transmission State



17.4.9 Smart card mode

Smart card mode is a single-line half-duplex communication mode. The interface supports ISO7816-3 standard protocol and can control the reading and writing of smart cards that meet the standard protocol.

SMEN bit of USART_CTRL5 register decides whether to enter the smart card mode.

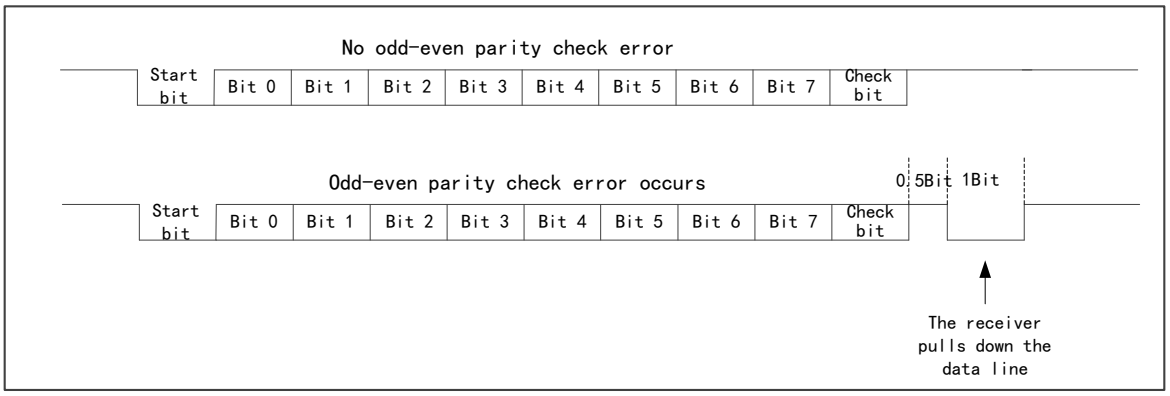
When USART enters the smart card mode:

- The LINEN bit of USART_CTRL3 register, and IRDAEN and HDMEN bits of USART_CTRL5 register must be cleared to 0.
- The data frame format is 8 data bits and 1 check bit, and 1.5 stop bits are used.
- CLKEN bit of USART_CTRL3 register can be set to provide clocks for smart card.
- During the communication, when the receiver detects a parity check error, in order to inform the transmitter that the data has not been

received successfully, the data line will be pulled down after half a baud rate clock, and keep pulling down for one baud rate clock.

- The break frame has no meaning in smart card mode. A 00h data with frame error will be regarded as a data instead of disconnection symbol.

Figure 57 ISO7816-3 Standard Protocol



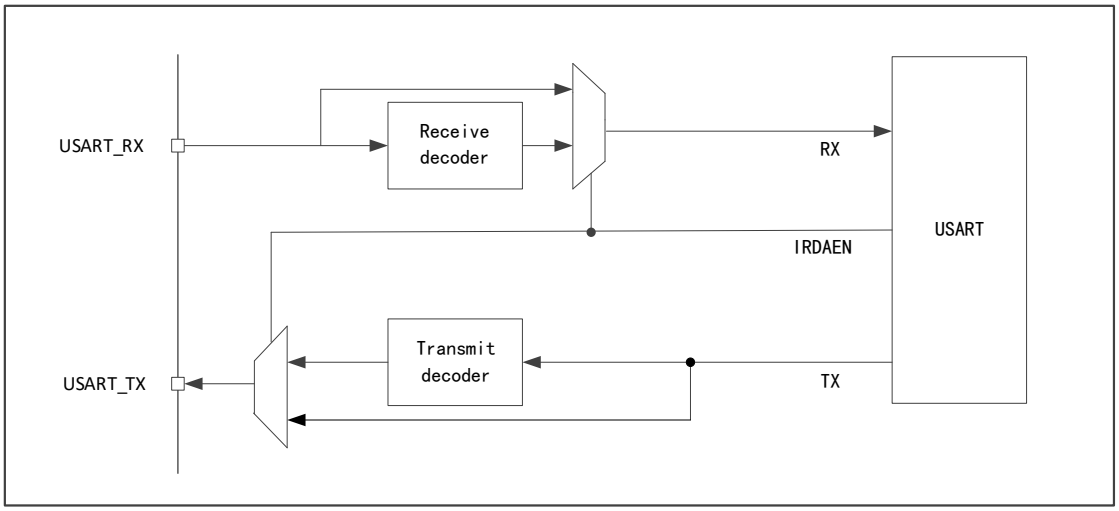
17.4.10 Infrared (IrDA SIR) function mode

IRDAEN bit of USART_CTRL5 register decides whether to enter the IrDA mode.

When USART enters the IrDA mode:

- The CLKEN, SBS and LINEN bits of USART_CTRL3 register, and HDMEN and SMEN bits of USART_CTRL5 register must be cleared to 0.
- The data frame uses 1 stop bit and the baud rate is less than 115200Hz.
- Using infrared pulse (RZI) indicates logic 0, so in normal mode, its pulse width is 3/16 baud rate cycles. In IrDA low-power mode, it is recommended that the pulse width be greater than three DIV frequency division clocks to ensure that this pulse can be detected by IrDA normally.

Figure 58 IrDA Mode Block Diagram



17.4.11 Low-power mode

Table 44 Low-power Mode of USART

Mode	Description
Wait mode (WAIT)	USART can monitor RX pin, and USART interrupt can wake up MCU
Standby mode (HALT)	Freeze USART register, and USART will fail to transmit and receive

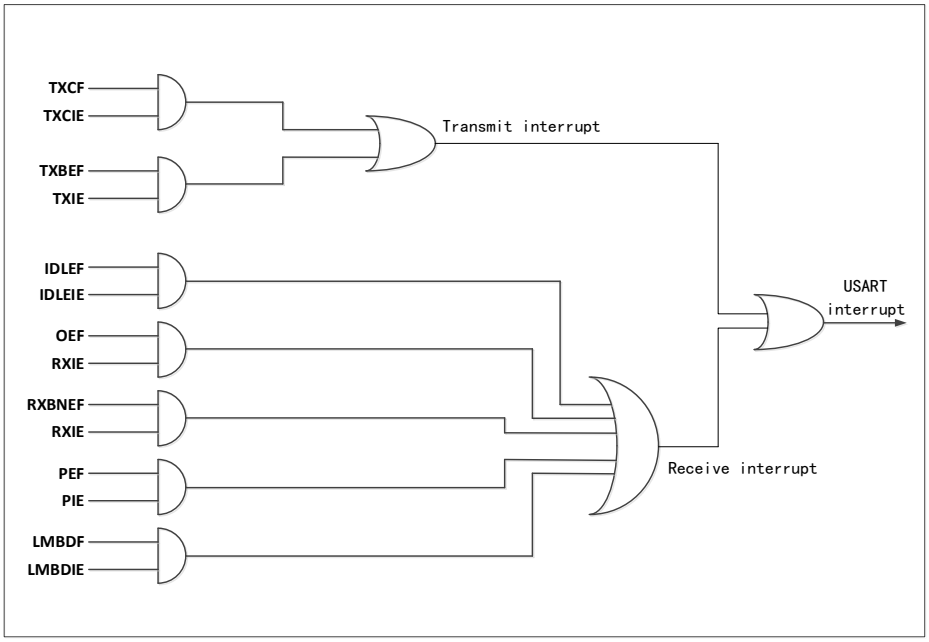
17.4.12 Interrupt request

Table 45 USART Interrupt Request

Interrupt event	Event flag bit	Enable bit
Data receiving completed	RXBNEF	RXIE
Overrun error	OEF	
Data transmit register is empty	TXBEF	TXIE
Transmission is completed	TXCF	TXCIE
Line idle is detected	IDLEF	IDLEIE
Parity check error	PEF	PIE
Break frame flag	LMBDF	LMBDIE

All interrupt requests of USART are connected to the same interrupt controller, and the interrupt requests have logical or relation before they are transmitted to the interrupt controller.

Figure 59 USART Interrupt Mapping



17.5 Register address mapping

Table 46 Register Address Mapping

Register name	Description	Offset address
USART_STS	State register	0x00
USART_DATA	Data register	0x04
USART_BR1	Baud rate register 1	0x08
USART_BR0	Baud rate register 0	0x0C
USART_CTRL1	Control register 1	0x10
USART_CTRL2	Control register 2	0x14
USART_CTRL3	Control register 3	0x18
USART_CTRL4	Control register 4	0x1C
USART_CTRL5	Control register 5	0x20
USART_GTS	Protection time setup register	0x24
USART_PSC	Prescaler register	0x28
USART_SW	Switch register	0x2C
USART_IOSW	I/O switch register	0x30

17.6 Register functional description

17.6.1 State register (USART_STS)

Offset address: 0x00

Reset value: 0x0000 00C0

Field	Name	R/W	Description
0	PEF	R	Parity Error Occur Flag 0: No error 1: Parity check error occurs In the receiving mode, when a parity check error occurs, set to 1 by hardware; This bit can be cleared to 0 by software; after setting of RXBNEF bit, first read USART_STS register, and then read USART_DATA register to complete clearing to 0.
1	FEF	R	Frame Error Occur Flag 0: No frame error 1: A frame error or disconnection symbol appears When there is synchronous dislocation, too much noise or disconnection symbol, set to 1 by hardware; This bit can be cleared to 0 by software; first read USART_STS register, and then read USART_DATA register to complete clearing to 0.
2	NEF	R	Noise Error Occur Flag 0: No noise 1: There is noise error When there is noise error, set to 1 by hardware; This bit can be cleared to 0 by software; first read USART_STS register, and then read USART_DATA register to complete clearing to 0.
3	OEF	R	Overrun Error Occur Flag 0: Overrun error 1: Overrun error occurs When the RXBNEF bit is set and the data in the shift register is to be transmitted to the receiver register, set to 1 by hardware; This bit can be cleared to 0 by software; first read USART_STS register, and then read USART_DATA register to complete clearing to 0.
4	IDLEF	R	IDLE Line Detected Flag 0: Idle bus is not detected 1: Idle bus is detected When idle bus is detected, set to 1 by hardware; This bit can be cleared to 0 by software; first read USART_STS register, and then read USART_DATA register to complete clearing to 0.
5	RXBNEF	RC_W0	Receive Data Buffer Not Empty Flag 0: The receive data buffer is empty 1: The receive data buffer is not empty When the data register receives the data transmitted by the receive shift register, set to 1 by hardware; This bit can be cleared to 0 by software; read USART_DATA to clear it to 0, or write 0 to this bit to clear it.

Field	Name	R/W	Description
6	TXCF	RC_W0	Transmit Data Complete Flag 0: Transmitting data is not completed 1: Transmitting data is completed After the last frame of data is transmitted and the TXBEF is set, set to 1 by hardware; This bit can be cleared to 0 by software; first read USART_STS register, and then write USART_DATA register to complete clearing to 0; or this bit can be cleared by writing 0 to it.
7	TXBEF	R	Transmit Data Buffer Empty Flag 0: The transmit data buffer is not empty 1: The transmit data buffer is empty When the shift register receives the data transmitted by the transmit data register, set to 1 by hardware; This bit can be cleared to 0 by software; write USART_DATA register to complete clearing to 0.
31:8	Reserved		

17.6.2 Data register (USART_DATA)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DATA	R/W	Data Value Transmit or receive the data value; read data when receiving data, and write data to the register when transmitting data.
31:8	Reserved		

17.6.3 Baud rate register 1 (USART_BR1)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DIV[11:4]	R/W	Fraction of USART Baud Rate Divider factor Bit 11 to bit 4 of division factor.
31:8	Reserved		

17.6.4 Baud rate register 0 (USART_BR0)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	DIV[3:0]	R/W	Fraction of USART Baud Rate Divider factor Lower four bits of division factor.
7:4	DIV[15:12]	R/W	Fraction of USART Baud Rate Divider factor Higher four bits of division factor.
31:8	Reserved		

17.6.5 Control register 1 (USART_CTRL1)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	PIE	R/W	Parity Error Interrupt Enable 0: Disable interrupt generation 1: Generate an interrupt when PEF is set
1	PSEL	R/W	Odd/Even Parity Selection 0: Even parity check 1: Odd parity check The selection will not take effect until the current transmission of bytes is completed.
2	PEN	R/W	Parity Control Enable 0: Disable 1: Enable If this bit is set, a check bit will be inserted in the most significant bit when transmitting data; when receiving data, check whether the check bit of the received data is correct. The check control will not take effect until the current transmission of bytes is completed.
3	WMS	R/W	Wakeup Method Configure 0: Idle bus wakeup 1: Address tag wakeup
4	DBL	R/W	Data Bits Length Configure 0: 1 start bit, 8 data bits, n stop bits 1: 1 start bit, 9 data bits, 1 stop bit This bit cannot be modified during transmission of data.
5	USARTDIS	R/W	USART Disable 0: Enable USART module 1: Disable USART frequency divider and output
6	TDB8	R/W	Transfer Data Bits8 When DBL=1, store the 9 bit of the transmitted data
7	RDB8	R/W	Receive Data Bits8 When DBL=1, store the 9 bit of the received data
31:8	Reserved		

17.6.6 Control register 2 (USART_CTRL2)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TXBRK	R/W	Transmit Break Frame 0: Not transmit 1: Will transmit This bit can be set by software and cleared to 0 by hardware when the stop bit of the break frame is transmitted.

Field	Name	R/W	Description
1	RMM	R/W	Receive Mute Mode Enable 0: Normal working mode 1: Mute mode This bit is set or cleared to 0 by software, or cleared to 0 by hardware when wakeup sequence is detected. USART must receive a data before it is put in the mute mode, so that it can be detected and awakened by idle bus. In the wake-up of address flag detection, if the RXBNEF bit is set, the RMM bit cannot be modified by software.
2	RXEN	R/W	Receive Enable 0: Disable 1: Enable, and start to detect the start bit on RX pin
3	TXEN	R/W	Transmit Enable 0: Disable 1: Enable Except in smart card mode, if there is a 0 pulse on this bit at any time of transmitting data, an idle bus will be transmitted after the current data is transmitted. After this bit is set, the data will be transmitted after delay of one-bit time.
4	IDLEIE	R/W	IDLE Interrupt Enable 0: Disable 1: Generate an interrupt when IDLEF is set
5	RXIE	R/W	Receive Buffer Not Empty Interrupt Enable 0: Disable 1: Generate an interrupt when OEF or RXBNEF is set
6	TXCIE	R/W	Transmit Complete Interrupt Enable 0: Disable 1: Generate an interrupt when TXCF is set
7	TXIE	R/W	Transmit Buffer Empty Interrupt Enable 0: Disable interrupt generation 1: Generate an interrupt when TXBEF is set
31:8	Reserved		

17.6.7 Control register 3 (USART_CTRL3)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	LBCP	R/W	Last Bit Clock Pulse Output Enable 0: Not output from CK 1: Output from CK
1	CLKPHA	R/W	Clock Phase Configure This bit indicates on the edge of which clock sampling is conducted 0: The first 1: The second

Field	Name	R/W	Description
2	CLKPOL	R/W	Clock Polarity Configure The state of CK pin when USART is in idle state 0: Low level 1: High level
3	CLKEN	R/W	Clock Enable (CK pin) 0: Disable 1: Enable
5:4	SBS	R/W	STOP Bit Configure 00: 1 stop bit 01: Reserved 10: 2 stop bits 11: 1.5 stop bits
6	LINEN	R/W	LIN Mode Enable 0: Disable 1: Enable
31:7	Reserved		

17.6.8 Control register 4 (USART_CTRL4)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	ADDR	R/W	USART Device Node Address Setup This bit is valid only in the mute mode of multiprocessor communication, and decides to enter the mute mode or wake up according to whether the detected address tags are consistent.
4	LMBDF	R/W	LIN Break Detected Flag 0: LIN disconnection not detected 1: LIN disconnection detected When LIN disconnection is detected, set to 1 by hardware; This bit can be cleared to 0 by software; or cleared by writing 0 to this bit.
5	LMBDL	R/W	LIN Break Detection Length Configure 0: 10 bits 1: 11 bits
6	LMBDIE	R/W	LIN Break Detection Interrupt Enable 0: Disable 1: Generate an interrupt when LMBDF bit is set
31:7	Reserved		

17.6.9 Control register 5\ (USART_CTRL5)

Offset address: 0x20

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	Reserved		

Field	Name	R/W	Description
1	IRDAEN	R/W	IrDA Function Enable 0: Disable 1: Enable
2	ILPM	R/W	IrDA Low-power Mode Enable 0: Normal mode 1: Low-power mode
3	HDMEN	R/W	Half-duplex Mode Enable 0: Disable 1: Enable
4	NACKEN	R	NACK Transmit Enable During Parity Error in Smartcard Function 0: NACK is not transmitted 1: Transmit NACK
5	SMEN	R	Smartcard Function Enable 0: Disable 1: Enable
31:6	Reserved		

17.6.10 Protection time setup register (USART_GTS)

Offset address: 0x24

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	GTS	R/W	Guard Time Value Setup After data are transmitted, TXCF can be set only after the protection time; the time unit is baud clock; which can be applied to smart card mode;
31:8	Reserved		

17.6.11 Prescaler register (USART_PSC)

Offset address: 0x28

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	PSC	R/W	Prescaler Factor Setup Divide the frequency of the system clock and provide the clock; in different working modes, the significant bits of PSC have difference, specifically as follows: In infrared low-power mode: PSC[7:0] is significant. 00000000: Reserved 00000001: 1 divided frequency 00000010: 2 divided frequency …… 11111111: 255 divided frequency In smart card mode: PSC[7:5] is insignificant, PSC[4:0] is significant 00000: Reserved 00001: 2 divided frequency

Field	Name	R/W	Description
			00010: 4 divided frequency 00011: 6 divided frequency …… 11111: 62 divided frequency
31:8	Reserved		

17.6.12 Switch register (USART_SW)

Offset address: 0x2C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SW	R/W	Open USART 0: Close USART 1: Open USART
31:1	Reserved		

Note: This register is only applicable to USART2 and USART3

17.6.13 I/O switch register (USART_IOSW)

Offset address: 0x30

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SW	R/W	Open USART IO Port 0: Close USART IO port 1: Open USART IO port
31:1	Reserved		

Note: This register is only applicable to USART3

18 Internal Integrated Circuit Interface (I2C)

18.1 Full Name and Abbreviation Description of Terms

Table 47Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Serial Data	SDA
Serial Clock	SCL
Clock	CLK
Negative Acknowledgement	NACK

18.2 Introduction

I2C is a short-distance bus communication protocol. In physical implementation, I2C bus is composed of two signal lines (SDA and SCL) and a ground wire. These two signal lines can be used for bidirectional transmission.

- Two signal lines, SCL clock line and SDA data line. SCL provides timing for SDA, and SDA transmits/receives data in series
- Both SCL and SDA signal lines are bidirectional
- The ground is common when the two systems use I2C bus for communication

18.3 Main characteristics

(1) Multi-master function

(2) The master can generate the clock, start bit and stop bit

(3) Slave function
- Programmable I2C address detection
- Detection of stop bit

(4) 7-bit and 10-bit addressing mode

(5) Response to broadcast

(6) Two communication speeds
- Standard mode
- Fast mode

(7) Programmable clock extension

(8) State flag
- Transmitter/Receiver mode flag
- Flag for end of byte transmission

- Busy bus flag

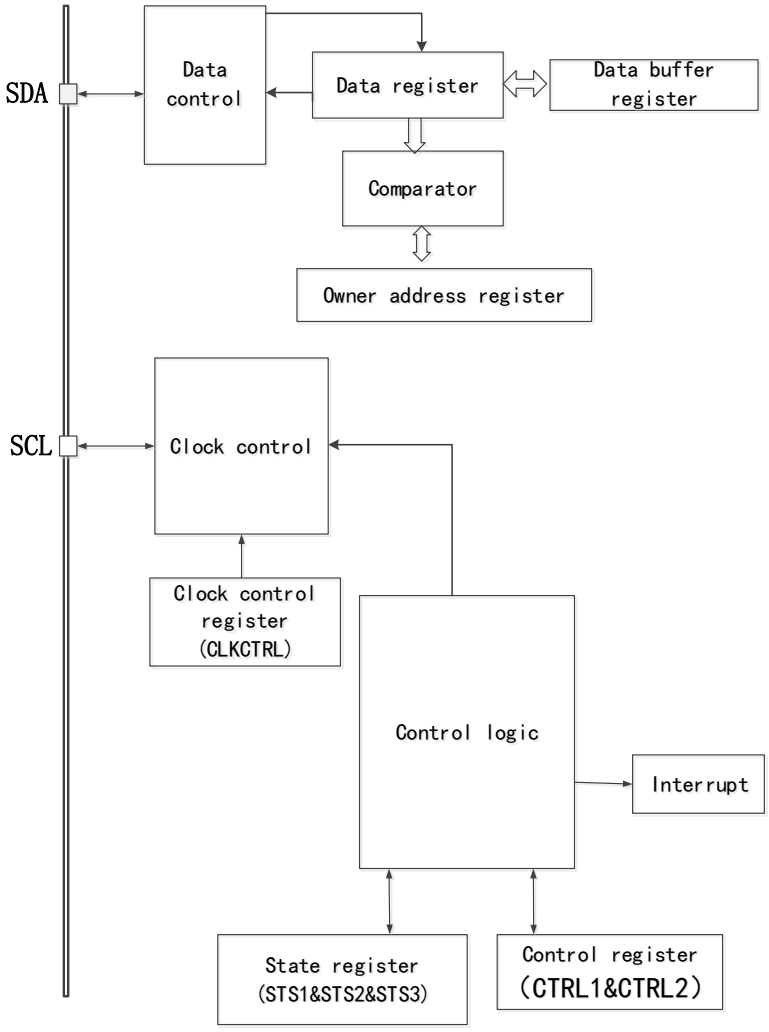
(9) Error flag
- Arbitration loss
- Acknowledgment error
- Detection of wrong start bit or stop bit

(10) Interrupt source
- Address/Data communication succeeded
- Error interrupt
- Wakeup interrupt

(11) Wakeup function
- The address matching detected in slave mode can wake up the MCU from low-power mode

18.4 Structure block diagram

Figure 60 I2C Functional Structure Diagram



The interface can be configured to the following modes:

- Slave transmitting
- Slave receiving
- Master transmitting
- Master receiving

In the initial state of I2C interface, the working mode is slave mode. After I2C interface transmits the start signal, it will automatically switch from slave mode to master mode.

18.5 Functional Description

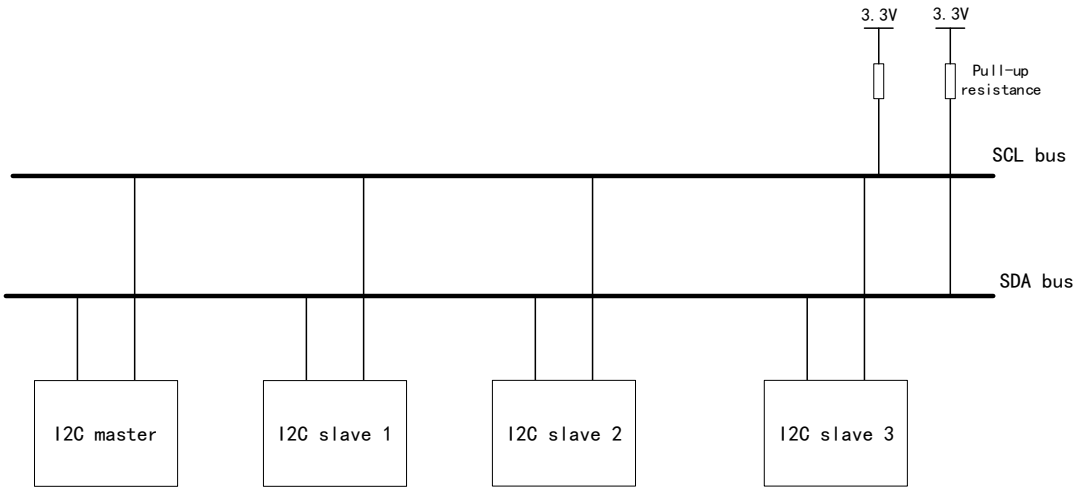
Table 48 Description of Proper Nouns of I2C Bus

Proper nouns	Description
Transmitter	Device transmitting data to the bus
Receiver	Device receiving data from the bus
Master	Device that initiates data transmission, generates clock signals and ends data transmission
Slave	Device addressed by master
Multiple masters	Multiple masters that control the bus at the same time without destroying information
Synchronization	The process of synchronizing the clock signals between two or more devices
Arbitration	If more than one master tries to control the bus at the same time, only one master can control the bus, and the information of the controlled master will not be destroyed

18.5.1 I2C physical layer

The commonly used connection modes between I2C communication devices are shown in the figure below:

Figure 61 Commonly Used I2C Communication Connection Diagram



Characteristics of physical layer:

(1) It supports the buses of multiple devices (signal line shared by multiple devices), which, in I2C communication bus, can connect multiple communication masters and communication slaves.

(2) An I2C bus only uses two bus lines, namely, a bidirectional serial data line (SDA) and a serial clock line (SCL). The data line is used for data transmission, and the clock line is used for synchronous receiving and transmission of data.

(3) Each device connected to the bus has an independent address (seven or ten bits), and the master addresses and accesses the slave device according to the address of the device.

(4) The bus needs to connect the pull-up resistor to the power supply. When I2C bus is idle, the output is in high-impedance state. When all devices are idle, the output is in high-impedance state, and the pull-up resistor pulls the bus to high level.

(5) Two communication modes: Standard mode (up to 100KHz) and fast mode (up to 400KHz).

(6) When the bus is used by multiple masters at the same time, to prevent data collision, the bus arbitration mode is adopted to determine which device occupies the bus.

(7) Can program setup and hold time, and program the high-level time and low-level time of SCL in I2C.

18.5.2 I2C protocol layer

Characteristics of protocol layer

(1) Data is transmitted in the form of frame, and each frame is composed of 1 byte (8 bits).

(2) In the rising edge phase of SCL, SDA needs to keep stable and SDA changes when SCL is low.

(3) In addition to data frame, I2C bus also has start signal, stop signal and acknowledgment signal.

- Start bit: During the stable high level period of SCL, a falling edge of SDA starts transmission.
- Stop bit: During the stable high level period of SCL, a rising edge of SDA stops transmission.
- Acknowledge bit: Used to indicate successful transmission of one byte. After the bus transmitter (regardless of the master or slave) transmits 8-bit data, SDA will release (from output to input). During the

ninth clock pulse period, the receiver will pull down SDA to respond to the received data.

I2C communication reading and writing process

Figure 62 Master Writes Data to Slave

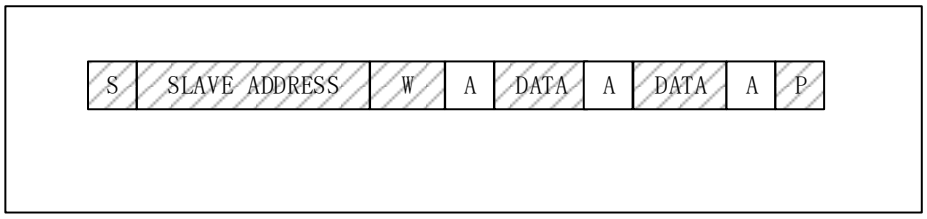
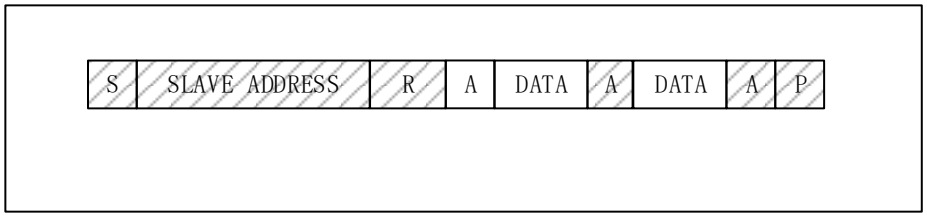


Figure 63 Master Reads Data from Slave



Remarks:

(1) : This data is transmitted from master to slave

(2) S: Start signal

(3) SLAVE ADDRESS: Slave address

(4) : This data is transmitted from slave to master

(5) R/W: Selection bit of transmission direction

(6) 1 means read

(7) 0 means write

(8) P: Stop signal

After the start signal is generated, all slaves will wait for the slave address signal transmitted by the master. In I2C bus, the address of each device is unique. When the address signal matches the device address, the slave will be selected, and the unselected slave will ignore the future data signal.

When the master direction is writing data

After broadcasting the address and receiving the acknowledgment signal, the master will transmit data to the slave, the data length is one byte, and every time the master transmits one byte of data, it needs to wait for the

acknowledgment signal transmitted by the slave. After all the bytes have been transmitted, the master will transmit a stop signal (STOP) to the slave, indicating that the transmission is completed.

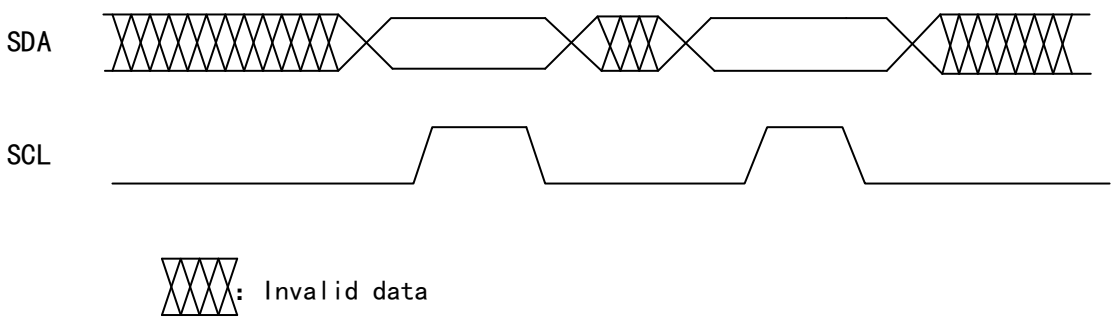
When the master direction is reading data

After broadcasting the address and receiving the acknowledgment signal, the slave will transmit the data to the master. The size of the data package is 8 bits. Every time the slave transmits one byte of data, it needs to wait for the acknowledgment signal from the master. When the master wants to stop receiving data, it needs to return a non-acknowledgment signal to the slave, then the slave will stop transmitting the data automatically.

18.5.3 Data validity

In the process of data transmission, the data on SDA line must be stable when the clock signal SCL is at high level. Only when the SCL is at the low level, can the level state of SDA be changed, and the bit transmission of each data needs a clock pulse.

Figure 64 SDA Timing Diagram



18.5.4 Start and stop signals

All data transmission must have start signal (START) and stop signal (STOP).

Figure 65 START signal is defined as: when SCL is at high level, SDA will convert from high level to low level

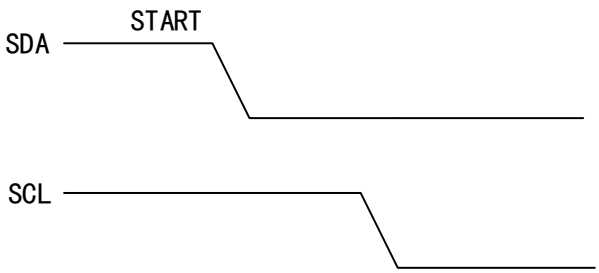
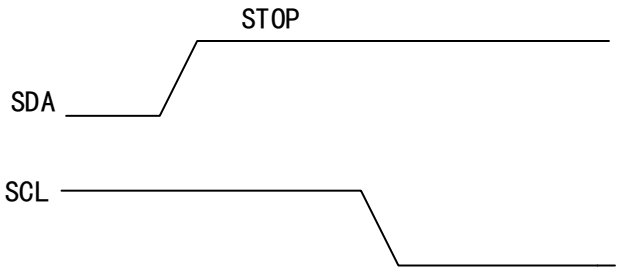


Figure 66 STOP signal is defined as: when SCL is at high level, SDA will convert from low level to high level



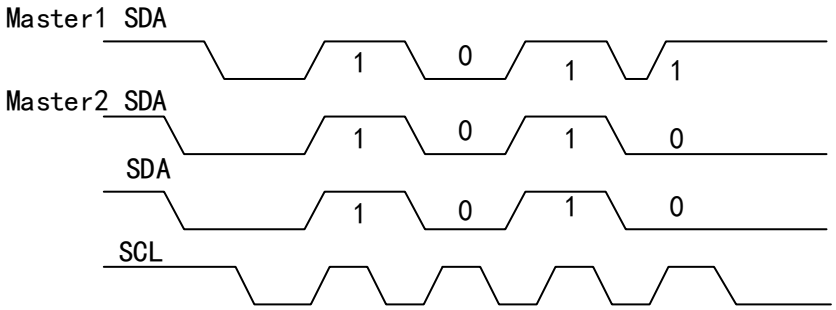
18.5.5 Arbitration

Arbitration is also used to solve the bus control conflict in case of multiple masters. The arbitration process takes place on the master and has nothing to do with the slave.

The master can start transmission only when the bus is idle. Two masters may generate an effective START signal on the bus within the shortest hold time of the START signal. In this situation, it is required that the arbitration should decide which master completes the transmission.

Arbitration is conducted by bit. During each arbitration, when SCL is high, each master will check whether the SDA level is the same as that transmitted by itself. The arbitration process needs to last for many bits. Theoretically, if two masters transmit exactly the same content, they can successfully transmit without arbitration failure. If one master transmits high level, but it is detected that SDA is at low level, an arbitration failure error will occur, the SDA output of the master will be closed, and the other master will complete its own transmission.

Figure 67 SDA Timing Diagram



Note: Master 1 arbitration failure

18.5.6 Error flag bit

Table 49 The following several error flag bits exist in I2C communication

Error flag bit	Description of error flag bit
Acknowledgment error flag bit (AEF)	No acknowledgment received

Bus error flag bit (BEF)	An external stop or start condition is detected
Arbitration loss flag bit (ALF)	Arbitration loss is detected by the interface
Overrun/Underrun error flag bit (OUF)	In slave mode, the received data is not read out, the next data has arrived, and an overrun error occurs. The transmitting data clock has arrived, but the data has not been written into the DATA register, and an underrun error occurs.

18.5.7 I2C interrupt

Table 50 I2C Interrupt Request

Interrupt event	Event flag bit	Interrupt control bit
Start bit transmission completed	SBTCF	EVTIE
Transmission completed/Address matching address signal	ADDRF	
10-bit address head segment transmission completed	ADDR10F	
Stop signal received signal	SBDF	
Data byte transmission completed	BTCF	
Wake up from the stop mode	WFHF	EVTIE
Receive buffer not empty	RXBNEF	EVTIE and BUFIE
Transmit buffer empty	TXBEF	
Bus error	BEF	ERRIE
Arbitration loss	ALF	
Answer failed	AEF	
Overrun/Underrun	OUF	

18.6 Register address mapping

Table 51 Register Address Mapping

Register name	Description	Offset address
I2C_CTRL1	Control register 1	0x00
I2C_CTRL2	Control register 2	0x04
I2C_CLKFREQ	Clock frequency register	0x08
I2C_ADDR0	Slave address register 0	0x0C
I2C_ADDR1	Slave address register 1	0x10
I2C_DATA	Data register	0x18
I2C_STS1	State register 1	0x1C
I2C_STS2	State register 2	0x20
I2C_STS3	State register 3	0x24

Register name	Description	Offset address
I2C_INTCTRL	Interrupt control register	0x28
I2C_CLKCTRL1	Master clock control register 1	0x2C
I2C_CLKCTRL2	Master clock control register 2	0x30
I2C_MRT	Rising time register	0x34

18.7 Register functional description

18.7.1 Control register 1 (I2C_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	I2CEN	R/W	I2C Enable 0: Disable 1: Enable
5:1	Reserved		
6	BCEN	R/W	Slave Responds Broadcast Enable 0: Disable 1: Enable Note: The broadcast address is 0x00
7	STRDIS	R/W	Slave Mode Clock Stretching Disable 0: Enable 1: Disable In slave mode, enabling extending the low-level time of the clock can avoid overrun and underrun errors.
31:8	Reserved		

18.7.2 Control register 2 (I2C_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	START	R/W	Start Bit Transfer This bit can be set to 1 and cleared to 0 by software; when transmitting the start bit or 2CEN=0, it is cleared to 0 by hardware. 0: Not transmit 1: Transmit
1	STOP	R/W	Stop Bit Transfer This bit can be set to 1 or cleared to 0 by software; when transmitting the stop bit, it is cleared to 0 by hardware; when timeout error is detected, it is set to 1 by hardware. 0: Not transmit 1: Transmit

Field	Name	R/W	Description
2	ACKEN	R/W	Acknowledge Transfer Enable This bit can be set to 1 or cleared to 0 by software; when I2CEN=0, it is cleared by hardware. 0: Not transmit 1: Transmit
3	ACKPOS	R/W	Acknowledge Position Configure This bit can be set to 1 or cleared to 0 by software; when I2CEN=0, it is cleared by hardware. 0: Whether transmitting NACK/ACK when receiving current byte 1: Whether transmitting NACK/ACK When receiving next byte
6:4	Reserved		
7	SWRST	R/W	Software Configure I2C under Reset State 0: Not reset 1: Reset; before I2C is reset, ensure that I2C pin is released and the bus is in idle state.
31:8	Reserved		

18.7.3 Clock frequency register (I2C_CLKFREQ)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
5:0	FREQ	R/W	I2C Clock Frequency Configure The clock frequency is the clock of I2C module, namely, the clock input from APB bus. 000000: Disable 000001: 1MHz 000010: 2MHz ... 011000: 24MHz 110000: 48MHz Others: Disable Minimum peripheral clock frequency required by I2C bus timing: 1MHz in the standard mode, and 4MHz in the fast mode.
31:6	Reserved		

18.7.4 Slave address register 0 (I2C_ADDR0)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	ADDR[0]	R/W	Slave Address Setup When the address mode is 7 bits, the bit is invalid; when the address mode is 10 bits, this bit is the 0 bit of the address.
7:1	ADDR[7:1]	R/W	Slave Address Setup The 7:1 bit of slave address
31:8	Reserved		

18.7.5 Slave address register 1 (I2C_ADDR1)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	Reserved		
2:1	ADDR[9:8]	R/W	Slave Address Setup When the address mode is 7 bits, the bit is invalid; when the address mode is 10 bits, this bit is the 9:8 bit of the address.
5:3	Reserved		
6	ADDRCFG	R/W	Address Mode Configure This bit is set to 1 by software.
7	ADDRMODE	R/W	Slave Address Mode Configure 0:7-bit address mode 1: 10-bit address mode
31:8	Reserved		

18.7.6 Data register (I2C_DATA)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DATA	R/W	Data Register In I2C transmission mode, write the data to be transmitted to this register; in I2C receiving mode, read the received data from this register.
31:8	Reserved		

18.7.7 State register 1 (I2C_STS1)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SBTCF	R	Start Bit Sent Finished Flag 0: Not transmit 1: Transmitted When the start bit is trasmitted, this bit can be set to 1 by hardware; this bit can be cleared after the software first reads STS1 register and then writes the DATA register; when I2CEN=0, it can be cleared to 0 by hardware.
1	ADDRF	R	Address Transfer Complete /Receive Match Flag Whether the matching address is received in slave mode: 0: Not received 1: Received Whether master mode address transmission is completed: 0: Not completed 1: Completed The bit is set to 1 by hardware; this bit can be cleared after the software first reads STS1 register and then reads STS3 register; when I2CEN=0, it can be cleared to 0 by hardware.

Field	Name	R/W	Description
2	BTCF	R	Byte Transfer Complete Flag 0: Not completed 1: Completed When receiving data, if failing to read the data received in DATA register, and a new data is received then, set to 1 by hardware; When transmitting data, if the DATA register is empty, set this bit to 1 by hardware to transmit the data in the shift register. This bit can be cleared after the software first reads STS1 register, and then reads or writes the DATA register; this bit can be cleared to 0 by hardware by transmitting a start bit and stop bit during the transmission, or when I2CEN=0.
3	ADDR10F	R	10-Bit Address Header Sent Flag 0: Not transmit 1: Transmitted The bit is set to 1 by hardware; this bit can be cleared after the software first reads STS1 register and then writes the DATA register; when I2CEN=0, it can be cleared to by hardware.
4	SBDF	R	Stop Bit Detection Flag 0: Not detected 1: Detected This bit can be cleared after the software first reads STS1 register and then writes CTRL2 register; when I2CEN=0, it can be cleared to 0 by hardware.
5	Reserved		
6	RXBNEF	R	Receive Buffer Not Empty Flag 0: The receive buffer is empty 1: The receive buffer is not empty This bit can be set to 1 by hardware when there is data in DATA register; This bit can be cleared after the software reads and writes DATA register; when I2CEN=0, it can be cleared to 0 by hardware.
7	TXBEF	R	Transmit Buffer Empty Flag 0: The transmit buffer is not empty 1: The transmit buffer is empty This bit can be set to 1 by hardware when the content of DATA register is empty; When the software writes the first data to the DATA register, it will immediately move the data to the shift register, then the data in the DATA register is empty and this bit cannot be cleared; This bit can be cleared after the software writes data to DATA register; after transmitting the start bit and stop bit, or when I2CEN=0, it can be cleared to 0 by hardware.
31:8	Reserved		

18.7.8 State register 2 (I2C_STS2)

Offset address: 0x20

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	BEF	RC_W0	Bus Error Flag 0: No bus error 1: Bus error occurred Bus error means exception of start bit or stop bit; when an error is detected, this bit can be set to 1 by hardware; this bit can be cleared after the software writes 0; when I2CEN=0, it can be cleared to 0 by hardware.
1	ALF	RC_W0	Master Mode Arbitration Lost Flag 0: No arbitration loss 1: In case of arbitration loss, I2C interface will automatically switch back to slave mode "Arbitration loss in master mode" means the master loses the control of buses; this bit is set to 1 by hardware; this bit can be cleared after the software writes 0; when I2CEN=0, it is cleared to 0 by hardware.
2	AEF	RC_W0	Acknowledge Error Flag 0: No acknowledgment error 1: Acknowledgment error occurred This bit can be set to 1 by hardware; this bit can be cleared after the software writes 0; when I2CEN=0, it can be cleared to 0 by hardware.
3	OUF	RC_W0	Overrun/Underrun Flag 0: Not occur 1: Occur This bit can be set to 1 by hardware when STRDIS=1 and one of the following conditions is met: (1) In the slave receiving mode, when the data in the DATA register is not read out, but a new data is received (this data will be lost), overrun occurs; (2) In the slave transmission mode, no data is written in the data register but it still needs to transmit data (the same data is transmitted twice), and then underrun occurs. This bit can be cleared by writing 0 by software; and cleared to 0 by hardware when I2CEN=0.
4	Reserved		
5	WFHF	RC_W0	Halt Mode Wakeup Flag 0: No wakeup from halt mode 1: Wakeup from stop mode This bit can be cleared by writing 0 by software; and cleared to 0 by hardware when I2CEN=0.
31:6	Reserved		

18.7.9 State register 3 (I2C_STS3)

Offset address: 0x24

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	MMF	R	Master Slave Mode Flag

Field	Name	R/W	Description
			0: Slave mode 1: Master mode This bit can be set to 1 by hardware when I2C is configured as master mode; This bit can be cleared to 0 by hardware when one of the following conditions is met: (1) Stop bit is generated (2) Bus arbitration is lost (3) I2CEN=0
1	BUSYF	R	Bus Busy Flag 0: The bus is idle (no communication) 1: The bus is busy (in the progress of communication) This bit can be set to 1 by hardware when SDA or SCL is at low level; and cleared to 0 by hardware after the stop bit is generated.
2	RWMF	R	Transmitter / Receiver Mode Flag 0: The device is in receiver mode (read) 1: The device is in transmitter mode (write) Decide the bit value according to R/W bit; This bit can be cleared to 0 by hardware when one of the following conditions is met: (1) Stop bit is generated (2) Repeated start bit is generated (3) Bus arbitration is lost (4) I2CEN=0
3	Reserved		
4	RBF	R	Slave Mode Received General Call Address Flag 0: Failed to receive the broadcast address 1: Broadcast address received This bit can be set to 1 by hardware; and cleared to 0 by hardware when one of the following conditions is met: (1) Stop bit is generated (2) Repeated start bit is generated (3) I2CEN=0
31:5	Reserved		

18.7.10 Interrupt control register (I2C_INTCTRL)

Offset address: 0x28

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	ERRIE	R/W	Error Interrupt Enable 0: Disable 1: Enable; when one bit of the following state registers is set to 1, an interrupt will be generated: OUF, AEF, ALF and BEF

Field	Name	R/W	Description
1	EVTIE	R/W	Event Interrupt Enable 0: Disable 1: Enable; when one bit of the following state register is set to 1, an interrupt will be generated: SBTCF, ADDRF, ADDR10F, SBDF, BTCF and WFHF
2	BUFIE	R/W	Buffer Interrupt Enable 0: Disable 1: Enable; when one bit of the following state register is set to 1, an interrupt will be generated: TXBEF and RXBNEF
31:3	Reserved		

18.7.11 Master clock control register 1 (I2C_CLKCTRL1)

Offset address: 0x2C

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	CLKCTRL[7:0]	R/W	Clock Setup in Fast/Standard Master Mode These bits are lower 8 bits of clock controller. In I2C standard mode: Thigh=CLKCTRL × T_{CK} Tlow=CLKCTRL × T_{CK} In I2C fast mode: When FMDC=0: Thigh=CLKCTRL×T_{CK} Tlow=2×CLKCTRL× T_{CK} When FMDC=1: Thigh=9 × CLKCTRL × T_{CK} Tlow=16 × CLKCTRL × T_{CK} Note: $t_{CK}=1/f_{CK}$, wherein f_{CK} is peripheral input clock configured by clock control register
31:8	Reserved		

18.7.12 Master clock control register 2 (I2C_CLKCTRL2)

Offset address: 0x30

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	CLKCTRL [11:8]	R/W	Clock Setup in Fast/Standard Master Mode These bits are higher 4 bits of clock controller. In I2C standard mode: Thigh=CLKCTRL × T_{CK} Tlow=CLKCTRL × T_{CK} In I2C fast mode: When FMDC=0: Thigh=CLKCTRL×T_{CK} Tlow=2×CLKCTRL× T_{CK} When FMDC=1: Thigh=9 × CLKCTRL × T_{CK} Tlow=16 × CLKCTRL × T_{CK}

Field	Name	R/W	Description
			Note: $t_{CK}=1/f_{CK}$, wherein f_{CK} is peripheral input clock configured by clock control register
5:4	Reserved		
6	FMDC	R/W	Fast Mode Duty Cycle Configure Here it is defined that the duty cycle=t_{low}/t_{high} 0: SCLK duty cycle is 1/3 1: SCLK duty cycle is 9/25
7	FASTMODE	R/W	Master Mode Speed Configure 0: Standard mode 1: Fast mode
31:8	Reserved		

18.7.13 Rising time register (I2C_MRT)

Offset address: 0x34

Reset value: 0x22C

Field	Name	R/W	Description
5:0	MRT	R/W	Master Mode Maximum Rise Time in Fast/Standard Mode The time unit is T_{CK}, and MRT is the maximum rising time of SCL plus 1.
31:6	Reserved		

19 Analog-Digital Converter (ADC)

19.1 Introduction

It is an ADC with 12-bit precision and can provide 8 multifunctional external input channels and 1 internal channel. In addition to supporting single-ended mode, the ADC also supports differential input mode, but Channel AIN8 only supports single-ended input mode. A/D conversion modes include single, continuous, buffered continuous, single scan and continuous scan. ADC conversion results can be left-aligned or right-aligned and stored in data register.

19.2 Main characteristics

(1) ADC power supply requirements: From 2.4V to 5.5V

(2) ADC input range: $V_{SS} \leq V_{IN} \leq V_{DD}$

(3) Conversion mode
- Single conversion mode
- Continuous conversion mode and buffered continuous conversion mode
- Single scan mode
- Continuous scan mode

(4) Channel category
- External GPIO input channel
- Internal input channel

(5) High performance
- Offset calibration
- Programmable prescaler
- Data alignment

(6) Interrupt
- Interrupt of end of conversion
- Analog watchdog interrupt

(7) Trigger mode
- External pin signal trigger
- Internal signal trigger generated by on-chip timer

(8) Analog amplification (VREF pin is required)

19.3 ADC functional description

19.3.1 ADC pins

Table 52 ADC Pins

Name	Description	Signal type
VDD	Power supply, positive ADC voltage, V_{DD}	Input, power supply
VSS	Power ground, V_{SS}	Input, power ground
VREF+	Positive A_{DC} reference voltage, connected to V_{DD} terminal	Input, analog reference power supply
VREF-	Negative A_{DC} reference voltage, connected to V_{SS} terminal	Input, analog reference power ground
AIN[8:0]	9 analog input channels	Analog input signal
ADC_ETR	External trigger signal	Digital input signal

19.3.2 Switch control

During the first ADC conversion, the ADCON bit shall be set to 1 twice. For the first time, the ADC wakes up from the low-power mode, and for the second time, the ADC conversion is started. After ADC conversion, it remains powered on. Then every time the ADCON bit is set, the conversion will be started once. If ADC conversion is not required in a short time, it is recommended to clear ADCON to zero and switch the ADC module to low-power mode.

19.3.3 ADC conversion mode

19.3.3.1 Single conversion mode

In this mode, for single channel, this channel can be switched once only. The channel to be converted can be selected by configuring CHSEL bit of ADC_CSTS register.

When the CCM bit of the ADC_CTRL1 configuration register is 0, ADC is set to single conversion mode; when the ADCON bit of ADC_CTRL configuration register is set to 1, ADC conversion starts.

After conversion of each channel, the conversion data will be stored in ADC_DATA register and CCF bit will be set to 1; if CCIE bit is set to 1, an interrupt will be generated.

19.3.3.2 Continuous conversion mode and buffered continuous conversion mode

In this mode, for single channel, only continuous conversion can be conducted for this channel.

When the CCM bit of the ADC_CTRL1 configuration register is set to 1, ADC is set to continuous conversion mode; when the ADCON bit of ADC_CTRL

configuration register is set to 1, ADC conversion starts.

- If the DBEN bit of ADC_CTRL3 register is set to 1, the buffer function will be enabled and the converted data will be stored in ADC_DATABUF buffer register; when the buffer register is filled up, the CCF bit will be set to 1; if the CCIE bit is set to 1, an interrupt will be generated and new conversion will start. If the data buffer register is overwritten before being read, the OVRF bit of ADC_CTRL3 register will be set to 1.
- If the DBEN bit of ADC_CTRL3 register is set to 0, the buffer function will be disabled, the converted data will be stored in ADC_DATA register, and the CCF bit will be set to 1; if the CCIE bit is set to 1, an interrupt will be generated and new conversion will start.

19.3.3.3 Single scan mode

This mode is used for conversion of a group of analog channels from AIN0 to AINn, and "n" is selected by the CHSEL bit of ADC_CSTS configuration register.

The scan mode can be enabled by setting the SMEN bit of ADC_CTRL2 configuration register to 1. When the CCM bit of the ADC_CTRL1 configuration register is 0, ADC is set to single conversion mode; when the ADCON bit of ADC_CTRL configuration register is set to 1, ADC conversion starts.

The single scan mode conversion starts from AIN0 channel, and the converted data will be stored in ADC_DATABUF buffer register; when the last channel conversion is completed, the CCF bit will be set to 1; i f the CCIE bit is set to 1, an interrupt will be generated. If the data buffer register is overwritten before being read, the OVRF bit of ADC_CTRL3 register will be set to 1.

19.3.3.4 Continuous scan mode

This mode is used for continuous conversion of a group of analog channels from AIN0 to AINn, and "n" is selected by the CHSEL bit of ADC_CSTS configuration register.

The scan mode can be enabled by setting the SMEN bit of ADC_CTRL2 configuration register to 1. When the CCM bit of the ADC_CTRL1 configuration register is set to 1, ADC is set to continuous conversion mode; when the ADCON bit of ADC_CTRL configuration register is set to 1, ADC conversion starts.

When the last channel conversion in the continuous scan mode is completed, a new scan conversion will automatically start from AIN0 channel. If the data buffer register is overwritten before being read, the OVRF bit of ADC_CTRL3 register will be set to 1.

19.3.4 ADC channel classification

19.3.4.1 Input channel introduced by GPIO pin

8 analog input channels: AIN0~AIN7

8 differential channels: VAIP0~VAIP3 and VAIN0~VAIN3

19.3.4.2 Internal input channel

1 internal channel is from on-chip VREF_BUFFER: AIN8

19.3.5 ADC differential function

ADC differential input only supports single mode, continuous mode and continuous mode with cache. Before ADC is enabled, set the DFS bit of ADC_CTRL4 configuration register to 1, select differential input, select the differential input channel by the CHSEL bit of ADC_CSTS configuration register, and other operations are the same as those of single-ended input. Note: The ADC differential mode does not support single-scan mode and continuous scan mode

Table 53 Correspondence of Differential Input Channels

Analog input	Pin
VAIP0/VAIN0	PC5/PC6
VAIP1/VAIN1	PC4/PD2
VAIP2/VAIN2	PD6/PD5
VAIP3/VAIN3	PD3/PC3

19.3.6 External trigger

The external trigger event can be selected by configuring ETS bit of ADC_CTRL2 register.

Table 54 External Trigger

Trigger source	ETS	Trigger type
TMR1_TRGO	00	Internal signal generated by on-chip timer
ADC_ETR	01	External pin

19.3.7 Analog watchdog

The analog watchdog is used to monitor whether the voltage on the corresponding pin exceeds the specified range. It usually uses single conversion mode and continuous mode without cache.

The analog watchdog can be enabled by setting the AWDIE bit of ADC_CSTS configuration register to 1. When the value exceeds the limited range of upper and lower limits after ADC conversion, set the AWDF bit to 1, indicating that an analog watchdog event occurred. The limited range of voltage is determined by

four registers, namely, ADC_AWDHT1, ADC_AWDHT0, ADC_AWDLT1 and ADC_AWDLT0.

When there are multiple channels that need to add the analog watchdog, the scan mode will be used, and the corresponding channels can be selected as the watchdog channel by setting the corresponding bit of ADC_AWDEN1 and ADC_AWDEN0 registers. If a watchdog event occurs to the channel, the corresponding bit of corresponding ADC_AWDS1 and ADC_AWDS0 registers will be set to 1, and the AWDF flag bit will be set at the same time. If the interrupt enable bit of AWDIE is 1, an interrupt will be generated at the end of a scanning sequence, and the AWDSx and AWDF bits must be cleared to zero in the interrupt subroutine.

To use continuous mode with cache, the method of the selected channel shall be the same as that of scan mode.

To reduce the waiting time after watchdog interrupt, it is recommended to put the analog watchdog channel at the last of the conversion sequence.

19.3.8 Data register

The data can be left-aligned or right-aligned, which is determined by DALIGCFG bit of configuration register ADC_CFG1; when DALIGCFG is set to 0, it means right-aligned, and if DALIGCFG is set to 1, it means left-aligned. The reading order of the data register is determined by the data alignment mode. In order to obtain correct results:

- In left-aligned mode, first read the high-byte register (ADC_DATA1), and then read the low-byte register (ADC_DATA0).
- In right-aligned mode, first read the low-byte register (ADC_DATA0)), and then read the high-byte register (ADC_DATA1).

19.3.9 Interrupt

Table 55 ADC Interrupt

Interrupt event	Event flag	Enable control
End of conversion	CCF	CCIE
Analog watchdog	AWDF	AWDIE

19.4 Register address mapping

Table 56 Register Address Mapping

Register name	Description	Offset address
ADC_DATABUFxH	ADC higher-bit data buffer register x	0x00+0x08*x
ADC_DATABUFxL	ADC lower-bit data buffer register x	0x04+0x08*x
ADC_CSTS	ADC control state register	0x80

Register name	Description	Offset address
ADC_CTRL1	ADC control register 1	0x84
ADC_CTRL2	ADC control register 2	0x88
ADC_CTRL3	ADC control register 3	0x8C
ADC_DATA1	ADC data register 1	0x90
ADC_DATA0	ADC data register 0	0x94
ADC_STD1	ADC Schmitt trigger disable register 1	0x98
ADC_STD0	ADC Schmitt trigger disable register 0	0x9C
ADC_AWDHT1	ADC analog watchdog high-threshold register 1	0xA0
ADC_AWDHT0	ADC analog watchdog high-threshold register 0	0xA4
ADC_AWDLT1	ADC analog watchdog low-threshold register 1	0xA8
ADC_AWDLT0	ADC analog watchdog low-threshold register 0	0xAC
ADC_AWDS1	ADC analog watchdog state register 1	0xB0
ADC_AWDS0	ADC analog watchdog state register 0	0xB4
ADC_AWDEN1	ADC analog watchdog enable register 1	0xB8
ADC_AWDEN0	ADC analog watchdog enable register 0	0xBC
ADC_CTRL4	ADC control register 4	0xC0
ADC_OFFSET	ADC offset register	0xC4

19.5 Register functional description

19.5.1 ADC higher-bit data buffer register x (ADC_DATABUFxH) (x=0..9)

Offset address: 0x00+0x08*x

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DATA	R	ADC Conversion High Data These bits are read-only. It includes higher-bit part of conversion results, which can only be used in buffered continuous mode and scan mode.
31:8	Reserved		

19.5.2 ADC lower-bit data buffer register x (ADC_DATABUFxL) (x=0..9)

Offset address: 0x04+0x08*x

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DATA	R	ADC Conversion Low Data These bits are read-only. It includes lower-bit part of conversion results, which can only be used in buffered continuous mode and scan mode.

Field	Name	R/W	Description
31:8	Reserved		

19.5.3 ADC control state register (ADC_CSTS)

Offset address: 0x80

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	CHSEL	R/W	Conversion Channel Select 0000: Analog channel AIN0 0001: Analog channel AIN1 …. 0111: Analog channel AIN7 1000: Analog channel AIN8 1001-1111: Reserved When DFS bit of ADC_CTRL4 register is set to 1, ADC will work in differential mode, and these bits are used to select differential input channel: 00xx: Channel VAIP0/Channel VAIN0 01xx: Channel VAIP1/Channel VAIN1 10xx: Channel VAIP2/Channel VAIN2 11xx: Channel VAIP3/Channel VAIN3
4	AWDIE	R/W	Analog Watchdog Interrupt Enable 0: Disable analog watchdog interrupt 1: Enable analog watchdog interrupt
5	CCIE	R/W	End Of Conversion Interrupt Enable 0: Disable the interrupt of end of conversion 1: Enable the interrupt of end of conversion
6	AWDF	RC_W0	Analog Watchdog Occur Flag 0: Not occur 1: Occur
7	CCF	R/W	End Of Conversion Flag 0: Not completed 1: Completed
31:8	Reserved		

19.5.4 ADC control register 1 (ADC_CTRL1)

Offset address: 0x84

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	ADCON	R/W	ADC Enable Write this bit and the ADC will wake up from the low-power mode and an ADC conversion will be triggered. If this bit is 0, after it is set to 1, the ADC will wake up from the low-power mode. If this bit is 1, after it is set to 1, AD conversion will start 0: Disable ADC conversion/calibration and enter the low-power mode 1: Enable ADC and start conversion

Field	Name	R/W	Description
1	CCM	R/W	Continuous Conversion Mode Enable 0: Single conversion mode 1: Continuous conversion mode
3:2	Reserved		
6:4	DIVSEL	R/W	Prescaler Select 000: $f_{ADC}=f_{MASTER}/2$ 001: $f_{ADC}=f_{MASTER}/3$ 010: $f_{ADC}=f_{MASTER}/4$ 011: $f_{ADC}=f_{MASTER}/6$ 100: $f_{ADC}=f_{MASTER}/8$ 101: $f_{ADC}=f_{MASTER}/10$ 110: $f_{ADC}=f_{MASTER}/12$ 111: $f_{ADC}=f_{MASTER}/18$
31:7	Reserved		

19.5.5 ADC control register 2 (ADC_CTRL2)

Offset address: 0x88

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	Reserved		
1	SMEN	R/W	Scan Mode Enable 0: Disable 1: Enable
2	Reserved		
3	DAM	R/W	Data Alignment Mode Configure 0: Right-aligned 1: Left-aligned
5:4	ETS	R/W	External Trigger Event Select 00: Internal timer 1 TRG event 01: External interrupt on ADC_ETR pin 10: Reserved 11: Reserved
6	ETEN	R/W	External Trigger Enable 0: Disable 1: Enable
31:7	Reserved		

19.5.6 ADC control register 3 (ADC_CTRL3)

Offset address: 0x8C

Reset value: 0x0000 0000

Field	Name	R/W	Description
5:0	Reserved		

Field	Name	R/W	Description
6	OVRF	RC_W0	Overrun Flag 0: No overrun occurs 1: Data overrun event is generated
7	DBEN	R/W	Data Butter Enable When this bit and CCM both are set to 1, the conversion result will exist in both ADC_DATABUFxH and ADC_DATABUFxL register. 0: Disable 1: Enable
31:8	Reserved		

19.5.7 ADC data register 1 (ADC_DATA1)

Offset address: 0x90

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DATA	R	ADC Conversion High Data These bits are read-only. It includes higher-bit part of conversion results, which can only be used when ADC is in single or non-buffer conversion mode.
31:8	Reserved		

19.5.8 ADC data register 0 (ADC_DATA0)

Offset address: 0x94

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	DATA	R	ADC Conversion Low Data These bits are read-only. It includes lower-bit part of conversion results, which can only be used when ADC is in single or non-buffer conversion mode.
31:8	Reserved		

19.5.9 ADC Schmitt trigger disable register 1 (ADC_STD1)

Offset address: 0x98

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	STD	R/W	Schmitter Triggers High Disable 0: Enable Schmitt trigger function 1: Disable Schmitt trigger function
31:8	Reserved		

19.5.10 ADC Schmitt trigger disable register 0 (ADC_STD0)

Offset address: 0x9C

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	STD	R/W	Schmitter Triggers Low Disable 0: Enable Schmitt trigger function 1: Disable Schmitt trigger function
31:8	Reserved		

19.5.11 ADC analog watchdog high-threshold register 1 (ADC_AWDHT1)

Offset address: 0xA

Reset value: 0x0000 00FF

Field	Name	R/W	Description
7:0	AWDHT	R/W	Analog Watchdog High Threshold High
31:8	Reserved		

19.5.12 ADC analog watchdog high-threshold register 0 (ADC_AWDHT0)

Offset address: 0xA4

Reset value: 0x0000 000F

Field	Name	R/W	Description
3:0	AWDHT	R/W	Analog Watchdog High Threshold Low
31:4	Reserved		

19.5.13 ADC analog watchdog low-threshold register 1 (ADC_AWDLT1)

Offset address: 0xA8

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	AWDLT	R/W	Analog Watchdog Low Threshold High
31:8	Reserved		

19.5.14 ADC analog watchdog low-threshold register 0 (ADC_AWDLT0)

Offset address: 0xAC

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	AWDLT	R/W	Analog Watchdog Low Threshold Low
31:4	Reserved		

19.5.15 ADC analog watchdog state register 1 (ADC_AWDS1)

Offset address: 0xB0

Reset value: 0x0000 0000

Field	Name	R/W	Description
1:0	AWDS[9:8]	RC_W0	Analog Watchdog Occur Flag High This bit is set to 1 by hardware and cleared to 0 by software. This register is used in buffered continuous conversion mode and scan mode. 0: Not occur 1: Occur
31:2	Reserved		

19.5.16 ADC analog watchdog state register 0 (ADC_AWDS0)

Offset address: 0xB4

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	AWDS[7:0]	RC_W0	Analog Watchdog Occur Flag Low This bit is set to 1 by hardware and cleared to 0 by software. This register is used in buffered continuous conversion mode and scan mode. 0: Not occur 1: Occur
31:8	Reserved		

19.5.17 ADC analog watchdog enable register 1 (ADC_AWDEN1)

Offset address: 0xB8

Reset value: 0x0000 0000

Field	Name	R/W	Description
1:0	AWDEN[9:8]	R/W	Analog Watchdog High Enable This bit can be set to 1 by hardware and cleared to 0 by software. This register is used in buffered continuous conversion mode and scan mode. 0: Disable 1: Enable
31:2	Reserved		

19.5.18 ADC analog watchdog enable register 0 (ADC_AWDEN0)

Offset address: 0xBC

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	AWDEN[7:0]	R/W	Analog Watchdog Low Enable This bit can be set to 1 by hardware and cleared to 0 by software. This register is used in buffered continuous conversion mode and scan mode. 0: Disable 1: Enable
31:8	Reserved		

19.5.19 ADC control register 4 (ADC_CTRL4)

Offset address: 0xC0

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	DISH	R/W	Differential Input Calibration 0: Normal 1: VIP and VIN are short-circuited inside, which offsets the calibration
1	GCMP	R/W	Internal Delay Time Select 0: f_{ADC}≥14MHz 1: f_{ADC}≤14MHz
2	DFS	R/W	Input Mode Select 0: Single-ended mode 1: Differential input Note: The differential mode does not support single-scan mode and continuous scan mode
31:3	Reserved		

19.5.20 ADC offset register (ADC_OFFSET)

Offset address: 0xC4

Reset value: 0x0000 0000

Field	Name	R/W	Description
5:0	OFFSET	R/W	Offset Configure Use complementary code to set 6-bit offset. 000000: 0-bit LSB offset 000001: +1-bit LSB offset ….. 011111: +31-bit LSB offset 100000: Reserved 100001: -31-bit LSB offset ….. 111111: -1-bit LSB offset
31:6	Reserved		

20 Chip Electronic Signature

The chip electronic signature includes Flash capacity information of main memory and 96-bit unique chip ID, which have been written into the system memory area of the chip before leaving the factory, and are read-only and cannot be modified by users.

20.1 Capacity register of main memory area

20.1.1 Flash capacity register (16 bits)

Base address: 0x0002 03E0

Read-only, the value has been prepared before leaving the factory

Field	Name	R/W	Description
31:0	F_SIZE	R	Flash Size Indicate the capacity of main memory area of the product (in KB). For example: 0x0020=32 Kbytes

20.2 96-bit unique chip ID

Purposes of unique ID may be:

- As serial number
- As a password; this unique identification can be used with software encryption and decryption algorithm to improve the security of the code in flash memory when writing the flash memory
- Used to activate the startup process with security mechanism
- The reference number provided by the identity label is unique to any MCU series. Users cannot change the unique ID under any circumstances. According to different usage, users can choose to read the identity label in byte, half word, or full word.

Offset address: 0x04

Read-only, the value has been prepared before leaving the factory

Field	Name	R/W	Description
31:0	U_ID[31:0]	R	Unique identity flag 31:0 bits

Offset address: 0x08

Read-only, the value has been prepared before leaving the factory

Field	Name	R/W	Description
31:0	U_ID[63:32]	R	Unique identity flag 63:32 bits

Offset address: 0x0C

Read-only, the value has been prepared before leaving the factory

Field	Name	R/W	Description
31:0	U_ID[95:64]	R	Unique identity flag 95:64 bits

21 Version History

Table 57 Document Version History

Date	Version	Version history
January, 2020	1.0	New
June 16, 2020	V1.0.1	Adjust the format
June 19, 2020	V1.0.2	Modify the timer description error
July 6, 2020	V1.0.3	Change the option byte description, and modify the cover format and contents and a register description error
February 15, 2022	V1.1	Modify the functional description
May 16, 2022	V1.2	Modify the TMR2/TMR4 predivision value in the register
June 22,2022	V1.3	(1) Modify Arm trademark (2) Add the statement
November 10, 2022	V1.4	(1) Delete the description of the systick divider (2) Example Change the address of a system storage area
March 16, 2023	V1.5	(1) Modify system block diagram (2) Modify the option byte size and supplement the option byte information (3) Modify the HIRC/24 in the clock source selection section of SYSCLK to HIRC/8 (4) Modify the description of the independent watchdog profile (5) Modify WWDT_ WDDATA 31:7 bit is reserved bit
December 5, 2023	V1.6	(1) Delete the description of downward counting and central alignment in the TMR2 chapter (2) Add communication peripherals for low power mode (3) Modify the "PWM output mode" section of the "PWM2 upward counting mode timing diagram" for advanced and universal timers (4) Modify power supply voltage

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8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.